Study of Force-Commutated Converter based HVDC System

By

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DEPARTMENT OF ELECTRICAL ENGINEERING

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A Thesis Submitted

in Partial Fulfilment of the Requirements

for the Degree of

Master of Technology

By

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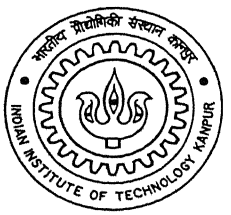

to

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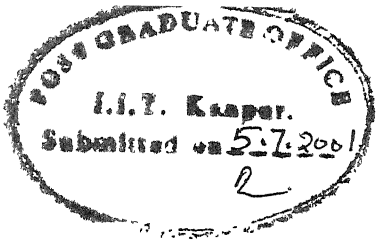

Certificate

It is certified that the work contained in the thesis entitled **Study of Force-Commutated Converter based HVDC System** by *Nitin Bansal* has been carried out under our supervision and that this work has not been submitted elsewhere for a degree.

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Last but not the least, I would like to thank almighty God, and my parents who made me to reach this stage, where I could undertake the work of this magnitude.

Nitin Bansal

Contents

Abstract

This thesis investigates in detail the suitable configuration, appropriate control scheme and a few applications of a force-commutated converter based HVDC systems. Initially, starting from the fundamental principles, a suitable configuration (from the point of view of harmonic generation) of the force-commutated converters for HVDC application is determined. Subsequently, two different application of force-commutated converter based HVDC systems are considered, namely, a) interconnection of two AC systems and b) feeding of isolated loads. Appropriate control schemes are proposed for these two applications. The effectiveness of the proposed control schemes is validated through detail digital transient simulation using PSCAD/EMTDC software

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Chapter 1

INTRODUCTION

Even though the alternating current (AC) transmission and distribution system is all-pervasive nowadays, it still suffers from some technical limitations. First, transmitting bulk amount of power over a long distance with AC transmission system is quite costly. Second, because of the right of way and economical bottlenecks, feeding a remote load center (which may be a remote village, mining center, isolated islands, gas and oil fields etc.) with AC supply proves to be quite difficult. Third, to meet the increasing demand of power in an environmental friendly way, more and more number of local, small scale, renewable power sources (such as wind, solar, tidal, bio-mass etc.) are being built to feed the remote local loads. However, the power output from these renewable sources varies significantly with time (in contrast with the constant power output from a synchronous generator). Thus, sometimes, it is possible that the remote loads may need extra power from the AC grid (because of the low power output from the renewable sources). Similarly, in other periods, when the power output from the renewable sources is high, it is equally possible that the renewable sources may need to export the extra amount of power (in excess of the local load demand) to the main AC grid. If the remote generation sites are connected to the main AC grid through AC interconnection, such bi-directional power flow over the AC line is not an easy task to accomplish. Fourth, as the AC network becomes more and more interconnected, the short circuit MVA at any point increases, thereby increasing the burden on the circuit breakers. Fifth, two AC networks operating asynchronously (i.e, having two different operating frequencies, e.g, 50.0 and 60.0 Hz.) can not be directly interconnected using an AC link. Sixth, in an AC interconnected system, the impact of any fault at any part of the grid is felt at almost all the other parts of the system to some lesser or greater extents.

To tackle the first, fourth, fifth and sixth problems, HVDC technology has been introduced, experimented with and nowadays is a mature technology [1]. Essentially, a HVDC system consists of two line-commutated converters (rectifier and inverter) with a DC link in between them. As the converters are line-commutated, presence of AC sources (of adequate short circuit MVA rating) at both the rectifier and inverter sides is an absolute necessity for their

commutation. Due to this reason, HVDC technology has been used very successfully to transmit bulk amount of power between two points within an existing AC network. However, due to this same reason, existing HVDC technology using line-commutated converters is not capable of supplying a remote, passive load as in that case, the AC source required for the commutation of the converter is absent at the inverter side. Because of the same reason, existing HVDC technology is not very suitable for exchanging power with the remote, small scale generations as the AC system at the inverter side (provided by the remote, renewable sources) may not have enough short circuit MVA to enable the commutation of the line-commutated converters. Moreover, the HVDC converters consume significant amount of reactive power from the adjacent AC network during their operation, which is also a cause for great concern.

To overcome the above limitations, the concept of force-commutated device (GTO) based HVDC system has been introduced in [2]. In [3], a GTO-based HVDC converter has been used to tap power from an existing two-terminal line-commutated converter based HVDC link. In [4], detail mathematical analysis of a self-commutated device based HVDC converter has been discussed. Recently, in [5]-[7], concepts and commercial implementation of world's first HVDC light transmission (small scale HVDC power transmission) have been described. Essentially, the converters used for HVDC light application are self-commutated device (such as GTO, IGBT etc.) based voltage source converters (VSC), which employ pulse-width modulation (PWM) switching technique. By means of the PWM switching technique, it is possible to generate AC voltage of any magnitude and phase (subject to the rating of the devices in the converter) at the output of the inverter. Thus, voltage source converters do not need the presence of any AC system for their commutation and hence, they are ideally suitable for supplying power to remote, isolated loads as well as for exchanging power with remote generations [5]-[7]. Moreover, as they can generate variable magnitude AC voltage at their AC side, voltage source converters can supply reactive power as well instead of consuming. However, because of the repeated `ON' and `OFF' switching of the devices, a lot of harmonics are generated from the converters, which are injected to the adjacent AC and DC systems. As high amount of harmonics deteriorates the `quality' of the power to an unacceptable level, it is absolutely necessary to ensure that the amount of harmonics generated from a converter is quite low, before the converters can be put into service. It is known that as the switching frequency of the converter increases, the amount of harmonics generated from them decreases [8]. On the other hand, the

switching frequency of GTOs for high power application is limited to a maximum ceiling of 500 Hz. Thus, the switching frequency of any GTO based VSC is also confined to a maximum limit of 500 Hz. Therefore, the amount of harmonics generated from a high power single PWM VSC may not be acceptably low. To overcome this difficulty, use of multi-bridge PWM converters has been proposed in the literature [9], where the effective switching frequency of the whole multi-bridge PWM converter is quite high while maintaining the switching frequency of individual converter within the maximum limit. Hence, multi-bridge PWM converters can be quite effective for practical implementation of force-commutated device based HVDC systems. However, none of the above papers [5]-[7] describes the details of the VSC used, the details of the PWM switching strategy employed and the detail of the control strategy implemented.

This thesis attempts to fill up the above gaps. Starting from the fundamental principle, a suitable configuration of the VSC employing an appropriate PWM switching technique is established first. Subsequently, different potential applications of the self-commutated converter based HVDC system are discussed and for each of these applications, suitable control strategies are proposed. The effectiveness of the proposed control strategies has been validated through detail digital transient simulation using PSCAD/EMTDC software package [10].

This thesis report is organized as follows. In Chapter 2, a suitable configuration of the self-commutated converter for HVDC application is established. In this chapter, it is demonstrated that for HVDC application, GTO based single PWM voltage source converter is not suitable. In Chapter 3, feasibility of transmission of power between two AC systems over a multi-PWM VSC based HVDC system is demonstrated. As discussed earlier, it is theoretically possible to supply a passive load by VSC based HVDC system, which, otherwise is not possible by line-commutated converter based HVDC system. Chapter 4 investigates the technical feasibility of supplying passive loads through multi-bridge PWM VSC based HVDC system. Finally, Chapter 5 discusses the main conclusions of this work and also delineates the scope of future research in this direction.

Chapter 2

SINGLE PWM VOLTAGE SOURCE CONVERTER BASED HVDC LINK

In this chapter, starting from the fundamental principle, the basic design of the configuration of a single voltage source converter (VSC) station for HVDC transmission is established initially. Subsequently, operation of a two terminal HVDC link involving a rectifier station and an inverter station is discussed.

2.1 Basic configuration of a single VSC station

The schematic diagram of a single converter station is shown in Fig. 2.1. The converter station essentially consists of the bridge converter, the converter reactor, the DC capacitor and an AC filter.

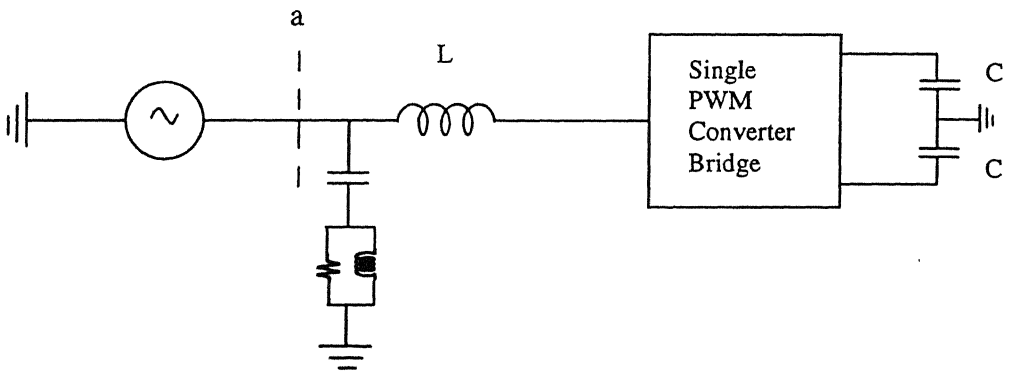

Fig 2.1 Single line diagram of a single converter station

The converter bridge being used here is a voltage source converter (VSC) instead of the phase-commutated converter (PCC), which is at present being used in the HVDC installations. Fundamentally, a VSC is comprised of self-commutated devices (such as GTO) that can both switch `ON' and switch `OFF' the current, whereas, a PCC is comprised of thyristors which can only switch `ON' the current and the current is switched `OFF' only at its natural zero crossing. In its basic form, the bridge has a two level, three phase topology with six valves and each valve

comprises of a number of GTOs in series. Every GTO is provided with an anti-parallel diode. The VSC was initially being used as an inverter but in mid eighties its use as a rectifier has been reported in literature [11]. This configuration when operated as a rectifier has shown to be capable of delivering near sinusoidal current waveform with unity or even leading power factor. Three-phase VSCs can provide constant dc bus voltage, low harmonic distortion of utility currents, bi-directional power flow, and controllable power factor. Since in a VSC the switching `OFF' of the current can be controlled, there is no need for an AC network to commutate against.

For switching the VSCs, the universally accepted method is to employ pulse width modulation (PWM) switching strategy. Various types of PWM techniques have been described in literature [8]. In this work, the sinusoidal PWM (SPWM) technique has been used. In SPWM technique, the switching pulse (`ON' or `OFF') is issued to the devices at the intersection of a reference signal and a high frequency carrier signal. In SPWM, the reference signal is a sinusoidal wave and hence is the name sinusoidal PWM technique. The high frequency carrier signal is a triangular wave having a frequency which is an integer multiple of the frequency of the reference signal. The frequency and phase of the reference signal determines the frequency and phase of the output voltage respectively and its peak amplitude controls the rms value of the output voltage. The ratio of the peak amplitude of the reference signal to that of the carrier wave is known as the modulation index. The devices are switched at a frequency equal to the frequency of the carrier wave. The schematic diagram of the SPWM switching strategy is shown in Fig. 2.2.

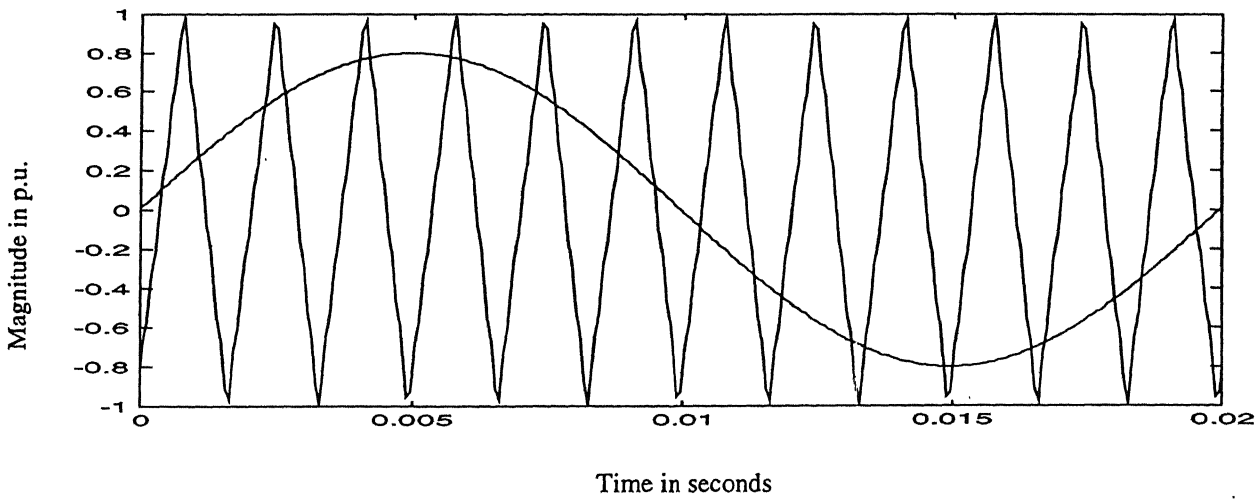

Figure 2.2: Schematic diagram of PWM switching technology

The converter reactor controls the active and reactive power flow between the converter and the AC network. Moreover, it also reduces the harmonics in the line current produced by the converter. The active power flow between the converter and the AC network is controlled by changing the phase angle (δ) between the fundamental frequency voltage generated by the converter (V_g) and the AC voltage (V_n) on the AC. bus. The active power flow between the converter and the network for a loss-less inductor is given by

$$P = \frac{V_g V_n Sin\delta}{X} \tag{2.1}$$

Similarly, the reactive power flow between the converter and the AC network is given by

$$Q = \frac{V_n\left(V_n - V_g Cos\delta\right)}{X} \tag{2.2}$$

Therefore, keeping everything else constant, a higher value of X reduces the amount of power exchanged between the AC bus and the converter, which is not very desirable. On the other hand, a higher value of X reduces the amount of harmonics in the line current, which is desirable. As these two objectives are conflicting, the value of the reactor should be chosen judiciously such that both the objectives are met simultaneously. The converter reactor can not eliminate the harmonics in the line current completely. Because of the presence of some amount of harmonics in the line current, the AC bus voltage also contains some amount of harmonics. These harmonics in the bus voltage are reduced by the AC filter. The objective of the DC capacitor is to primarily serve as an energy storage device to be able to control the power flow. The capacitor also reduces the harmonics on the DC side. As the value of the DC capacitor increases, the harmonics on the DC side decreases, but the capacitor charging becomes slower. Hence, the value of the DC capacitor also needs to be chosen carefully so as to comply with both these conflicting objectives simultaneously and satisfactorily.

For satisfactory operation of the converter station, the values of the reactor, DC capacitor as well as the parameters of the AC filter must be chosen very carefully. In the next section, the methodology for choosing the different appropriate values is described in detail.

2.2 Design of a single VSC station

For determining the various appropriate values of the different components as discussed above, a single, stand-alone VSC station has been chosen and is being operated as a rectifier. When the VSC station is operating as a rectifier, the basic objective is to charge the DC capacitor. For charging the capacitor, active power must flow from the AC side to the converter. To achieve this, it is observed from equation (2.1) that V_g must lag V_n by some appropriate angle. As the angle of V_g is determined by the angle of the reference wave of the SPWM technique, the DC capacitor can be charged by maintaining the phase of the reference wave at some lagging value with respect to the AC voltage. For the purpose of determining the appropriate values of different components, the phase of the reference wave has been maintained at an angle of 5° (lagging) with respect to the AC voltage. The frequency of the triangular carrier wave has been fixed at 450 Hz and the modulation index has been assumed to be 0.8.

Initially, the appropriate value of the DC capacitor has been chosen. For this purpose, the value of converter reactor has been fixed arbitrarily at 0.2 H and digital simulation studies have been carried out with three different values of the DC capacitor (5μF, 25μF and 100μF). The simulation results are shown in Fig. 2.3, where the variation of DC voltage is depicted. It is to be noted that Figs. 2.3(a), (b) and (c) correspond to capacitor values 100μF, 25μF and 5μF respectively. It is to be observed from this figure that for all the cases, the DC capacitor voltage reaches the same level (180 kV). However, the harmonic content in the DC voltage for a capacitor value of 100μF is much lower than in the cases with capacitor values 25μF and 5μF. Hence, for further studies, the value of the DC capacitor has been fixed at a value of 100μF.

After the DC capacitor value is fixed, simulation studies have been carried out to determine the appropriate value of the converter reactor. Towards this objective, keeping the value of the DC capacitor fixed at 100μF, three different values of the converter reactor, namely 0.1H, 0.2H and 0.3H have been chosen and digital simulation studies have been carried out for all these three cases. The simulation results are shown in Figs. 2.4, 2.5 and 2.6 respectively. Each of these figures shows the plot of the variation of the DC capacitor voltage (in part a), plot of the line current for one cycle (in part b) and the result of Fourier analysis of the line current (in part c). It is to be noted that the results corresponding to reactor values 0.1H, 0.2H and 0.3H are shown in Figs. 2.4, 2.5 and 2.6 respectively. It can be observed from these figures that for reactor value of 0.1H, the harmonics in the line current is highest and the DC capacitor voltage reaches

its steady state value most quickly. On the other hand, for a reactor value of 0.3H, the harmonics in the line current is lowest but the rate of rise of the DC capacitor voltage is lowest. Thus, to compromise between these two criteria (i.e. harmonics in the line current and rate of rise of DC capacitor voltage), the converter reactor value has been fixed at 0.2 H.

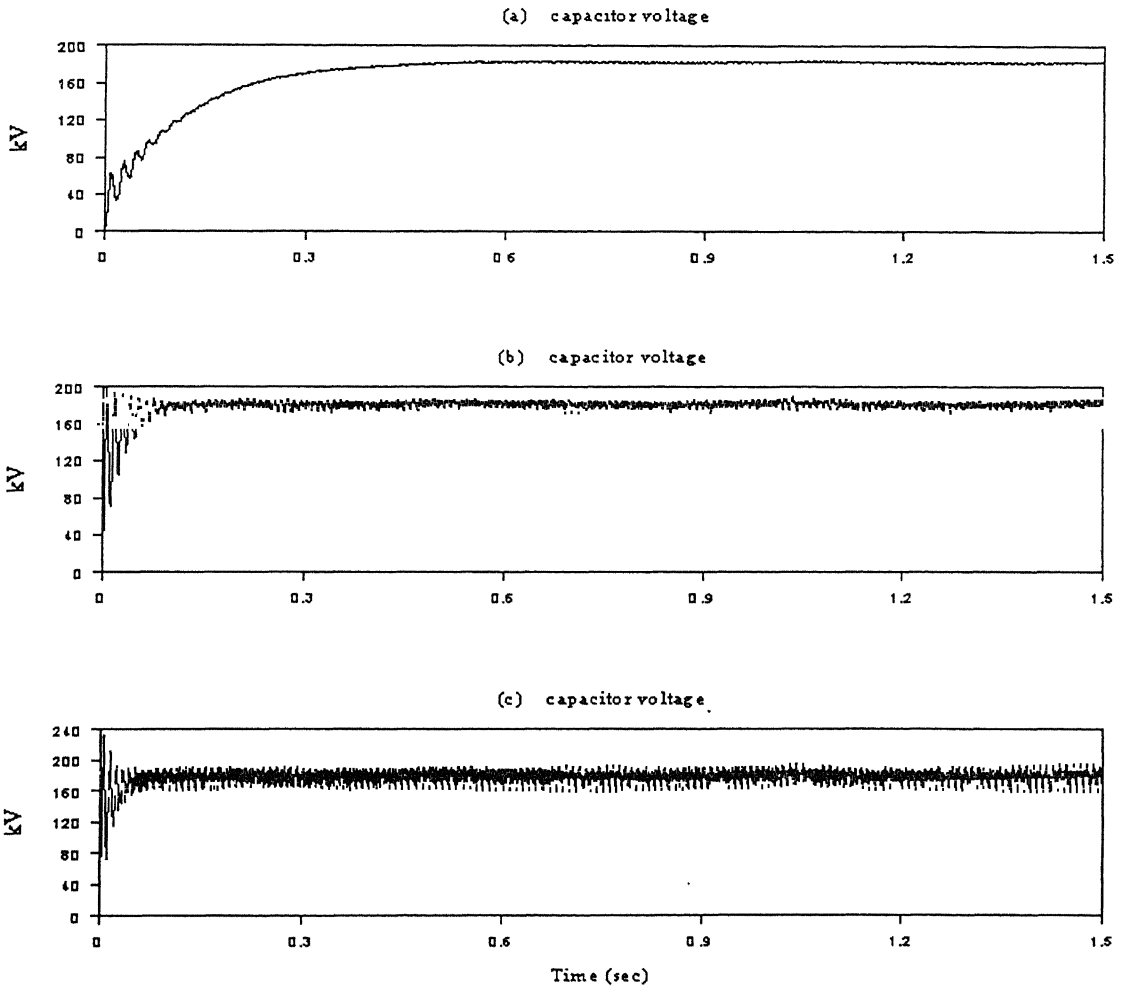

Figure 2.3 : Simulation results with different capacitor values.

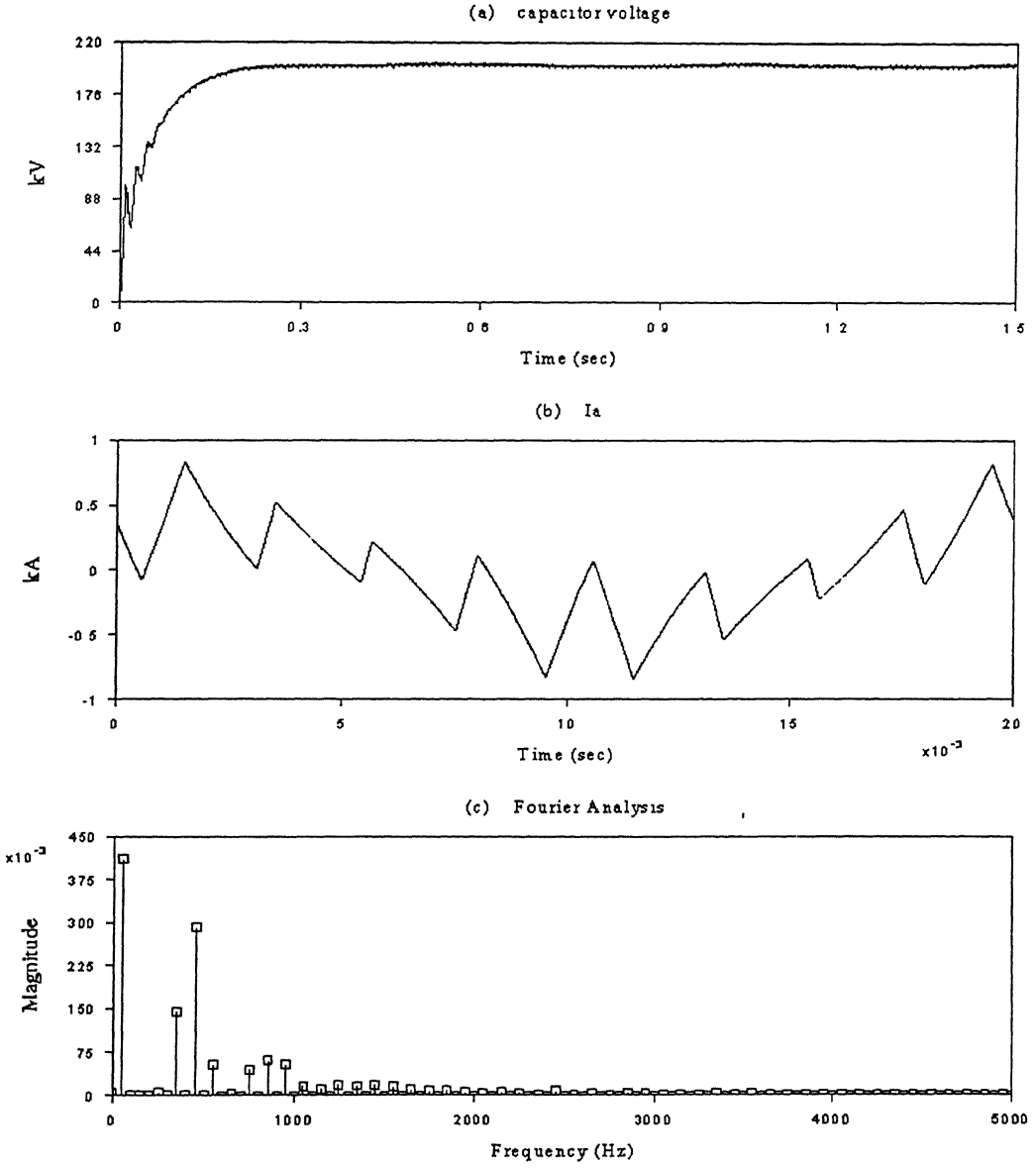

Figure 2.4: Simulation results with converter reactor = 0.1H and DC capacitor = 100μF

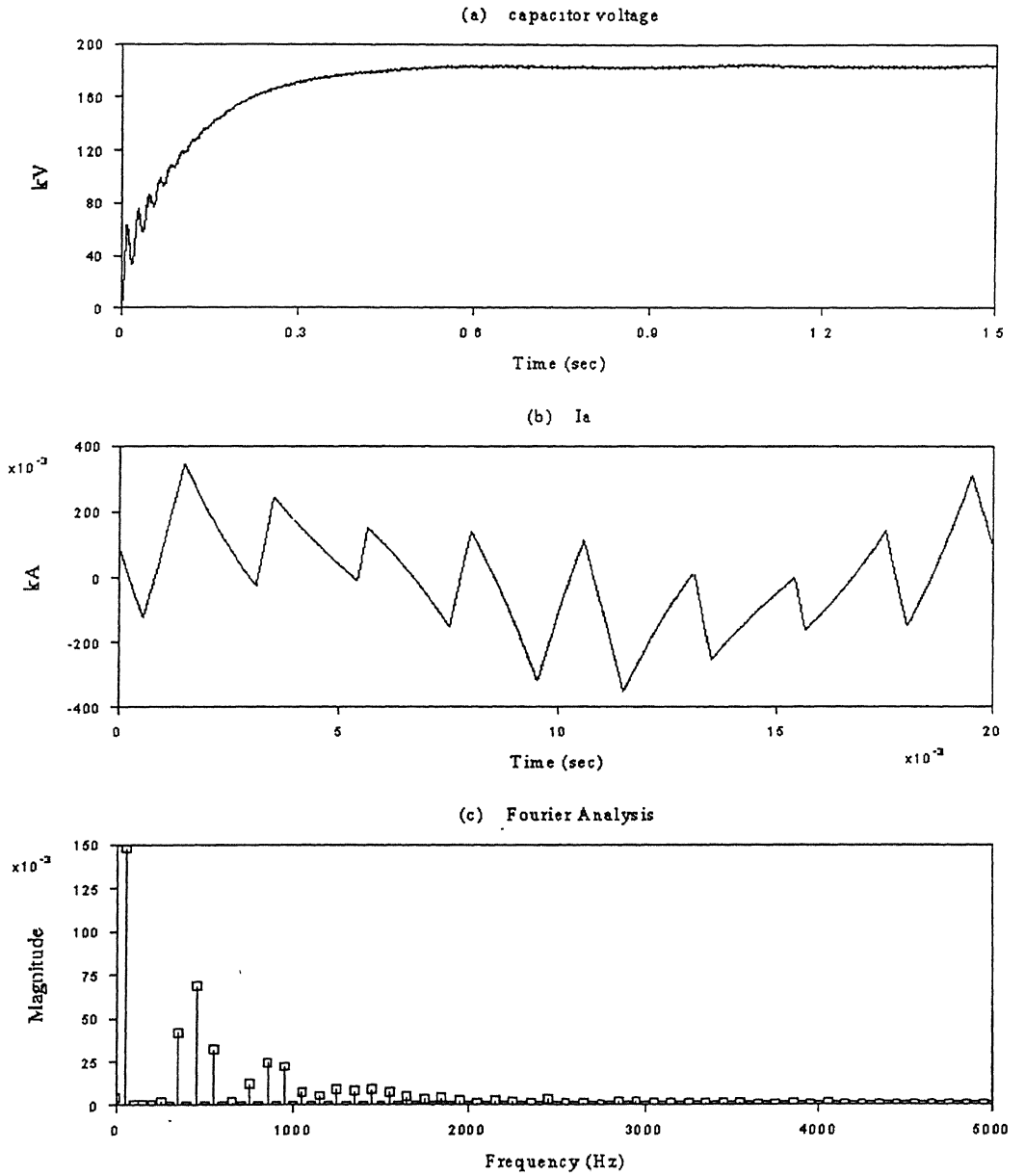

Figure 2.5: Simulation results with converter reactor = 0.2H and DC capacitor = 100μF

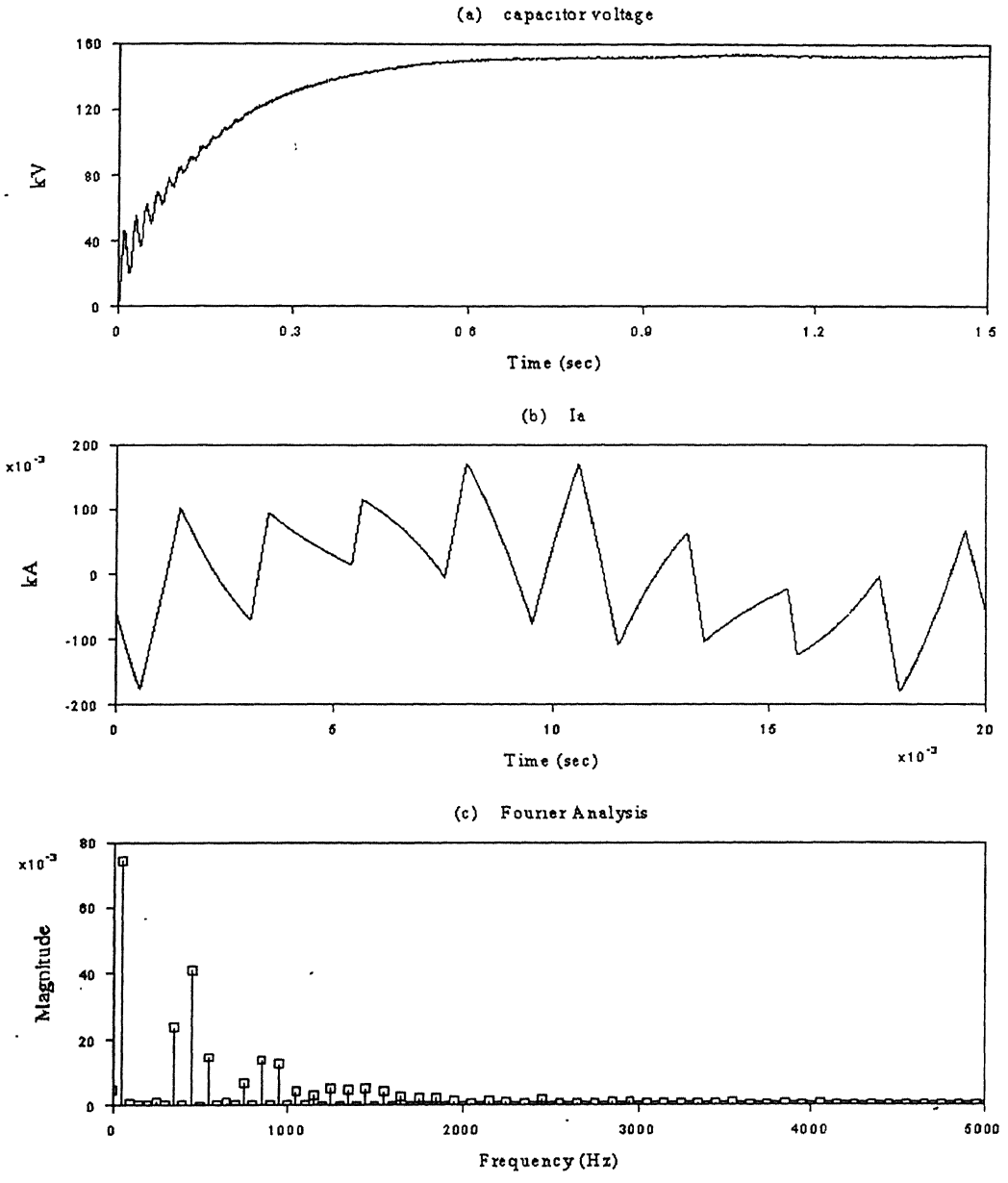

Figure 2.6: Simulation results with converter reactor = 0.3H and DC capacitor = 100μF

After the values of these two components are fixed, it is necessary to determine the appropriate value of the switching frequency. According to [5]-[7], the switching frequency of the devices should be restricted to 2 kHz. It is also known that as the switching frequency increases, the harmonic contents in the system decreases. To verify this, digital simulation studies have been performed with three different switching frequencies, namely, 450 Hz, 900 Hz and 1800 Hz. In each of these cases, the converter reactor values has been kept fixed at 0.2H and that of the DC capacitor at 100μF. The simulation results are shown in Figs. 2.7, 2.8 and 2.9 respectively. In each of these results, line current for one cycle (part a), its Fourier analysis (part b), a-phase voltage for one cycle at point `a' in Fig. 2.1 (part c) and its Fourier analysis (part d) are shown. Figs. 2.7, 2.8 and 2.9 correspond to switching frequencies 450 Hz, 900 Hz. and 1800 Hz. respectively. From these figures it is observed that the harmonic content is lowest for a switching frequency of 1800 Hz. Hence, for subsequent studies, the switching frequency has been fixed at 1800 Hz.

From the above figures it is clearly observed that when the stand-alone rectifier is operating at an operating frequency of 1800 Hz., most of the harmonics in the line current are eliminated. However, still a significant amount of harmonics is present in the system voltage. To remove these voltage harmonics, AC filters (as shown in Fig. 2.1) have been connected to the system and steady state operating condition has again been obtained. The filters used are of the shunt type. They are the tuned high pass filters, with the filter parameters as follows : quality factor = 10 and cut-off frequency = 1700Hz. The simulation results with these harmonic filters connected in the system are shown in Fig. 2.10. From this figure it is clearly observed that most of the harmonics in the voltage have been removed by the filter.

Once all the above parameters have been fixed, a two-terminal HVDC link having two identical converter stations on each side (rectifier and inverter) has been considered. The parameters at each station have been fixed at the values established above. The schematic diagram of the HVDC link is shown in Fig. 2.11. The parameters of the transformers and the sources at both the ends in Fig. 2.11 are given in the Appendix. A resistance of 10.0 ohm with a series inductance of 0.025 H has been assumed to represent the DC link. This reactance represents the aggregate value of the DC link resistance as well as the two small smoothing reactors at the two sides of the DC link. For successful operation of the HVDC link, proper control strategy must be developed. As discussed earlier, the objective of the rectifier side VSC

is to charge the DC side capacitor and maintain its voltage at a constant level. The voltage of the DC capacitor depends upon the amount of active power flow between the AC side and the converter station, which, in turn, depends on the relative phase of the reference wave of the SPWM technique with respect to the AC side voltage. Thus, the DC capacitor voltage can be controlled by controlling the phase of the reference wave and hence, a proportional-integral (PI) controller, as shown in Fig. 2.12, has been used to control the rectifier side DC capacitor voltage. The value of the proportional gain (Kp) has been chosen to be 0.0 while the value of the integral gain (K_i) has been chosen as 10.0. The value of the DC voltage reference has been assumed to be 160 kV in this work. Thus, the responsibility of voltage control of the HVDC link has been entrusted to the rectifier side in this control philosophy. Consequently, the responsibility of controlling the DC current or power is to be entrusted with the inverter side. In this work, the inverter side has been used to control the amount of active power to be transferred to the inverter AC side. Again, the amount of active power to be transferred to the inverter AC side depends on the relative phase difference between the reference wave of the inverter VSC station and the inverter side AC voltage. Thus, another PI controller as shown in Fig. 2.13 has been used to control the inverter side active power. The values of the proportional gain (Kp) and the integral gain (Ki) have been chosen to be 0.0 and 2.0 respectively for both these controllers. A value of 50 MW has been assumed as the reference power setting for this inverter side PI controller.

With the above two controllers in place, digital simulation studies have been carried out. The results at the steady state operating condition are shown in Fig. 2.14. In this figure, the response of the rectifier side PI controller (part a), traces of rectifier side DC capacitor voltage (part b), response of the inverter side PI controller (part c), and the trace of the inverter side active power (part d) are shown. From this figure, it is clearly observed that the proposed controllers are able to maintain the DC capacitor voltage and the inverter side active power at their reference values. For further investigation into the operation of this two terminal link at steady state, the traces of one cycle of `a' phase current at the rectifier side (part a), its Fourier spectrum (part b), one cycle of `a' phase voltage at point `a' (refer to Fig. 2.1) at the rectifier side (part c) and its Fourier spectrum (part d) are shown in Fig. 2.15. From this figure, it is observed that there is negligible amount of harmonics in the system.

Although acceptable performance has been obtained from the two-terminal HVDC link operating at 1800 Hz., in practice, for high power application, the maximum switching frequency

of a GTO is limited to 500 Hz. Consequently, it is not practically feasible to operate a HVDC link with single PWM converters at both the sides having a switching frequency of 1800 Hz.. To overcome this difficulty, application of multi-bridge PWM converters in two-terminal HVDC link is presented in the next chapter.

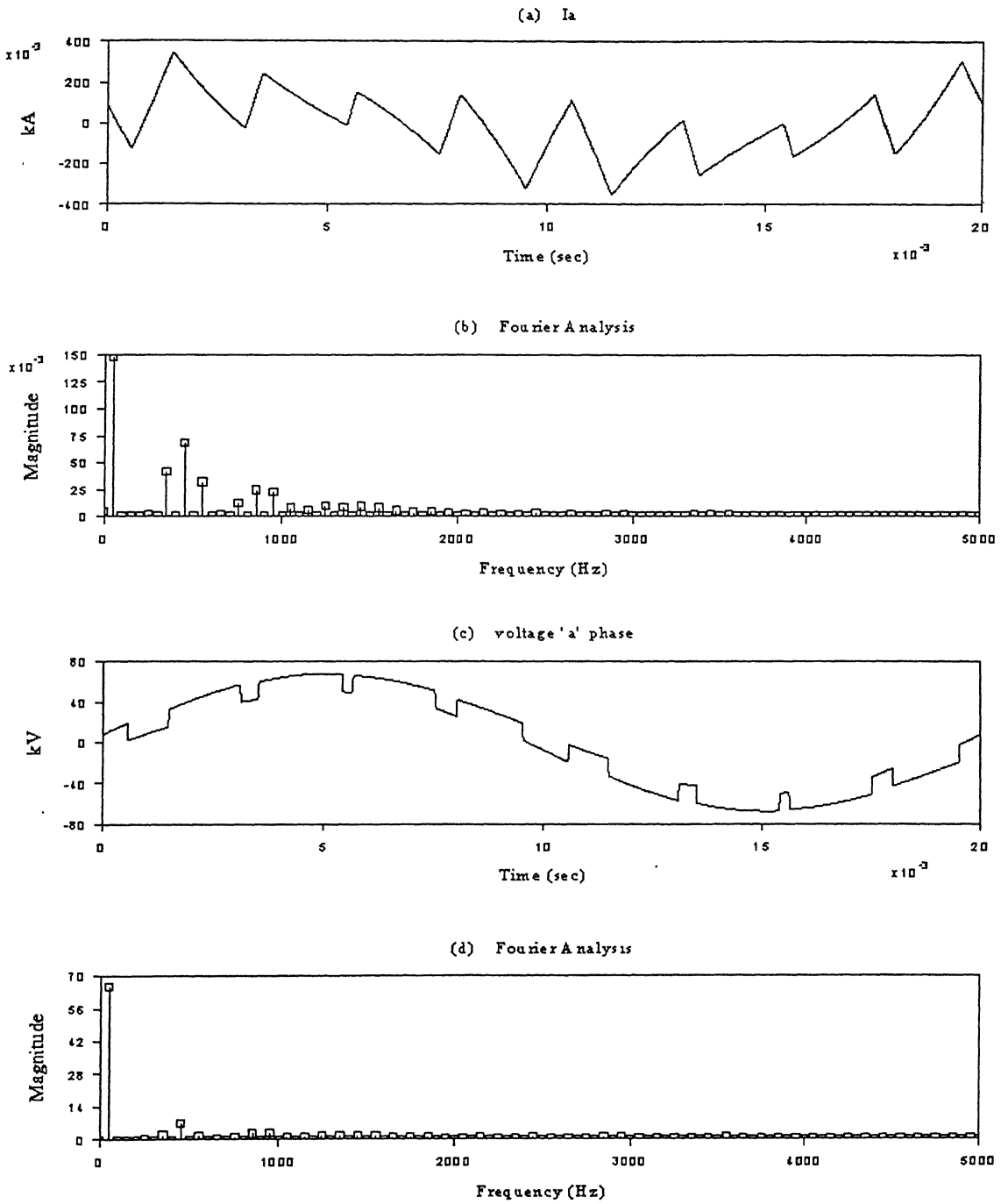

Figure 2.7: Simulation results for switching frequency = 450Hz

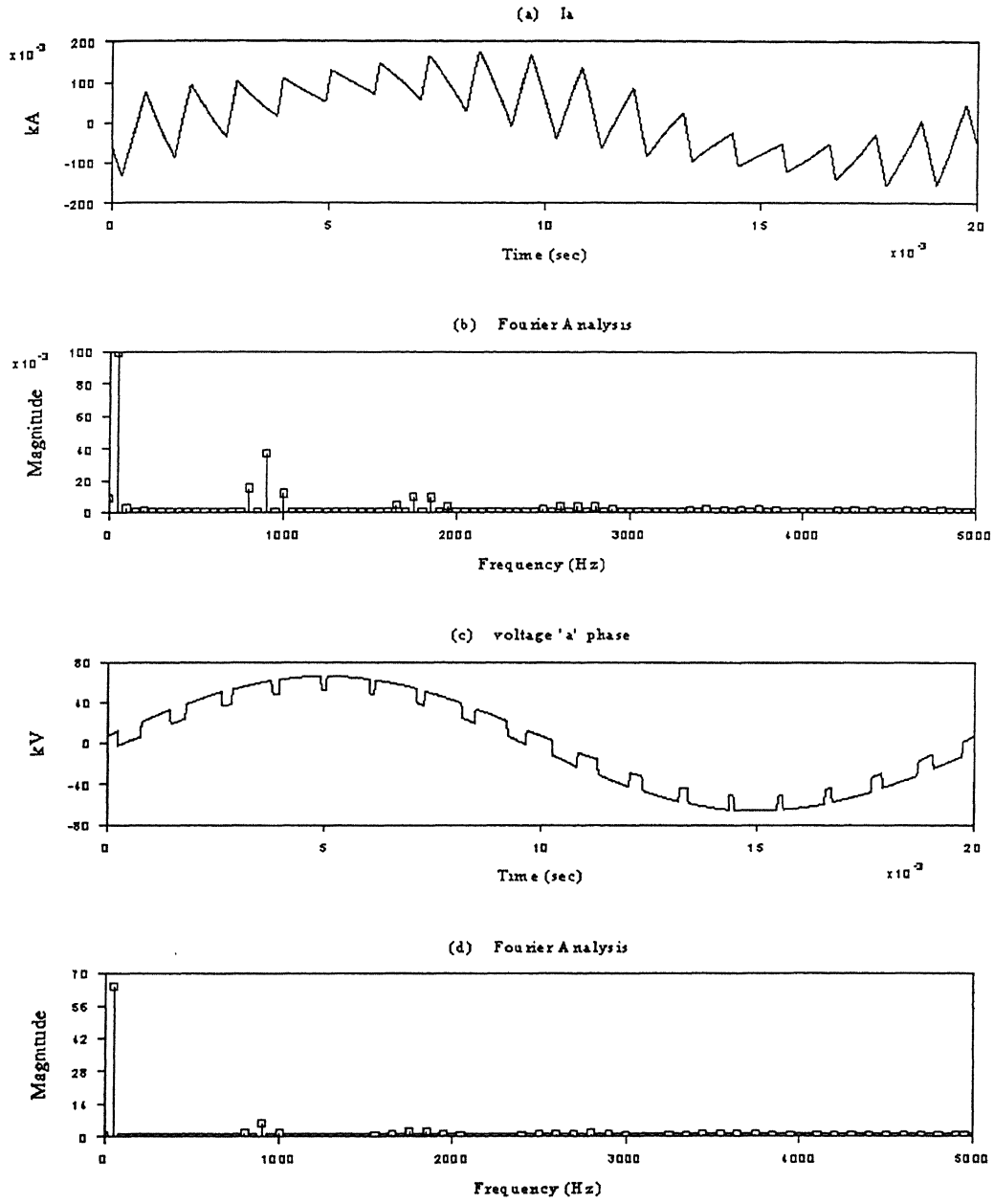

Figure 2.8: Simulation results for switching frequency = 900Hz

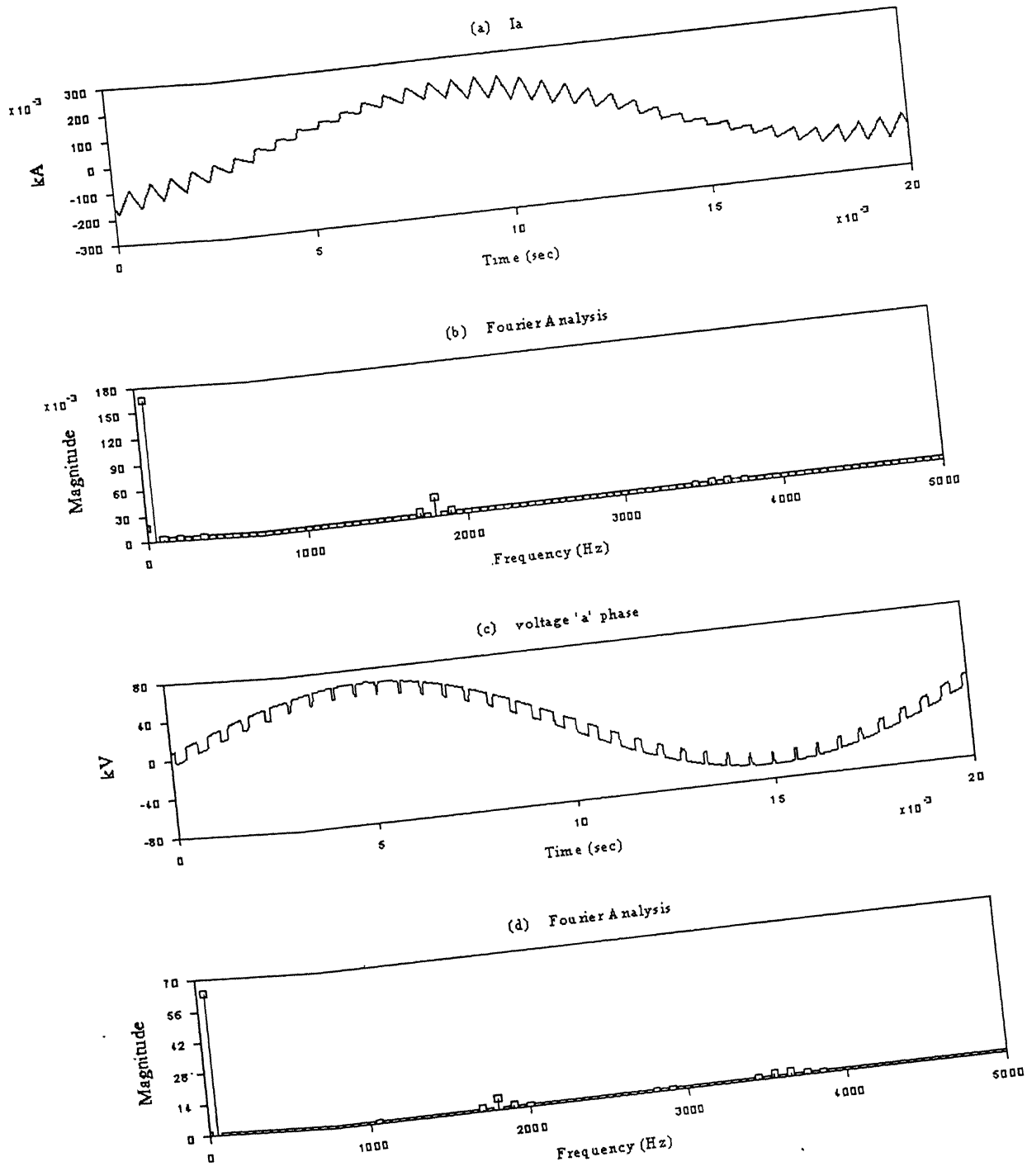

Figure 2.9: Simulation results for switching frequency = 1800Hz

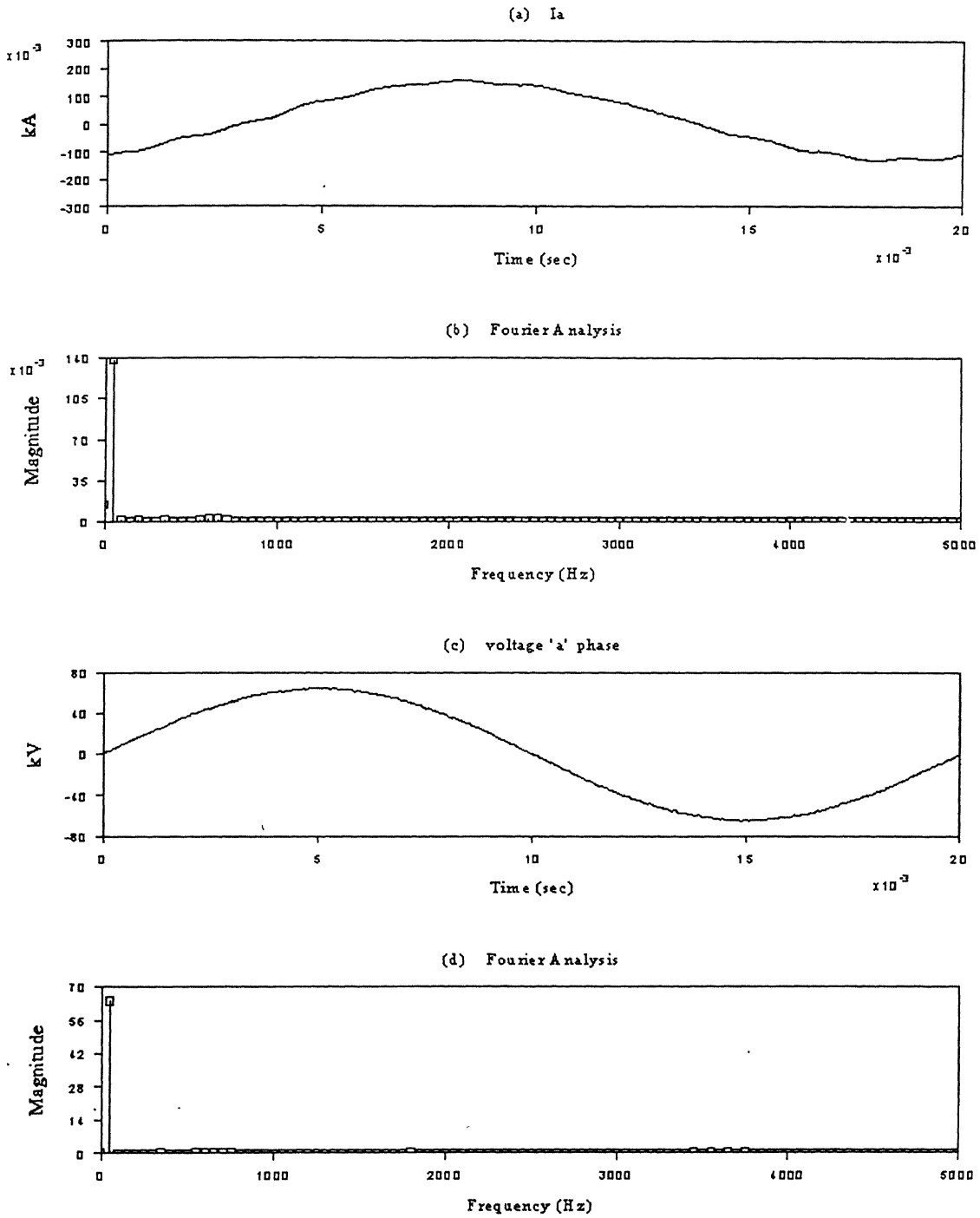

Figure 2.10: Simulation results for stand-alone rectifier with filters.

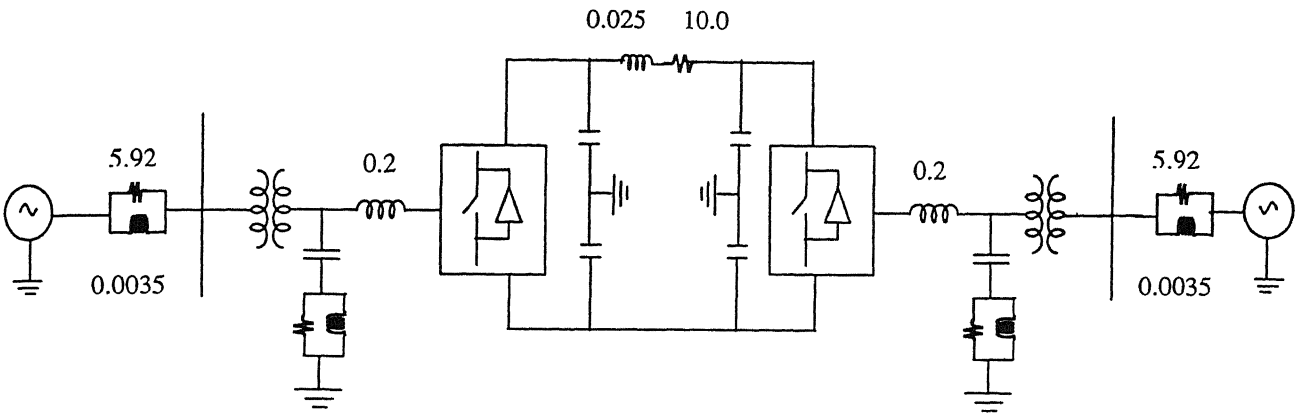

Figure 2.11: Schematic diagram of a two terminal DC link using Single PWM converter

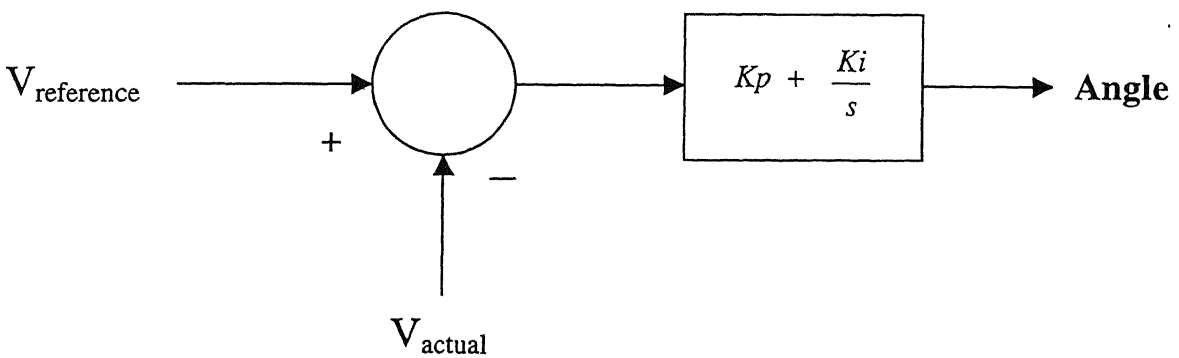

Figure 2.12: Schematic diagram of PI controller on the rectifier side

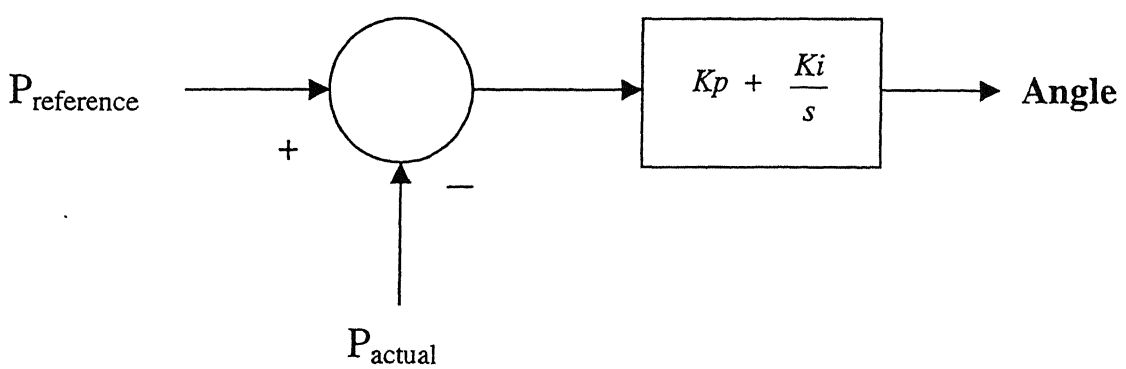

Figure 2.13: Schematic diagram of PI controller on the inverter side

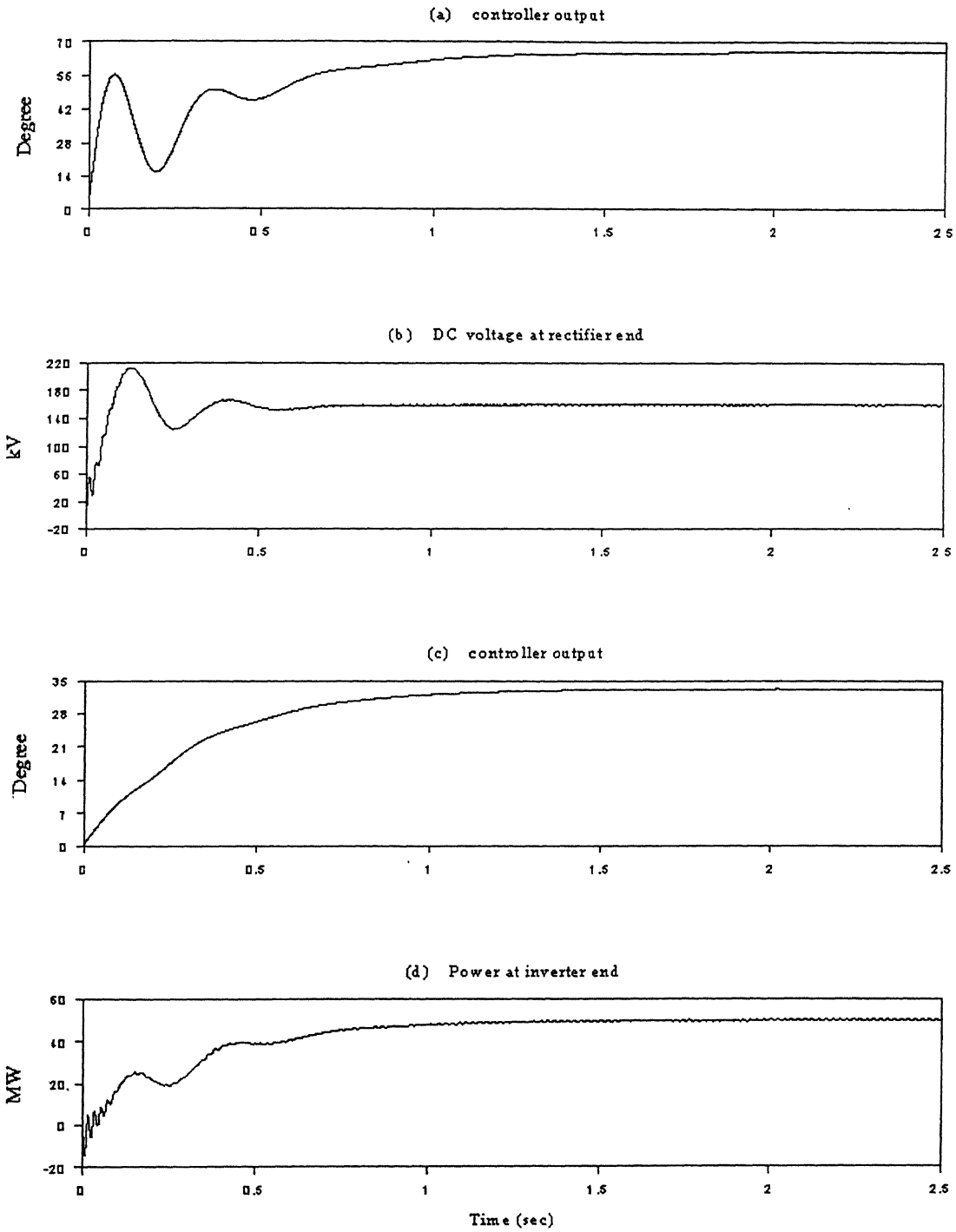

Figure 2.14: Steady state operation of a two terminal DC link

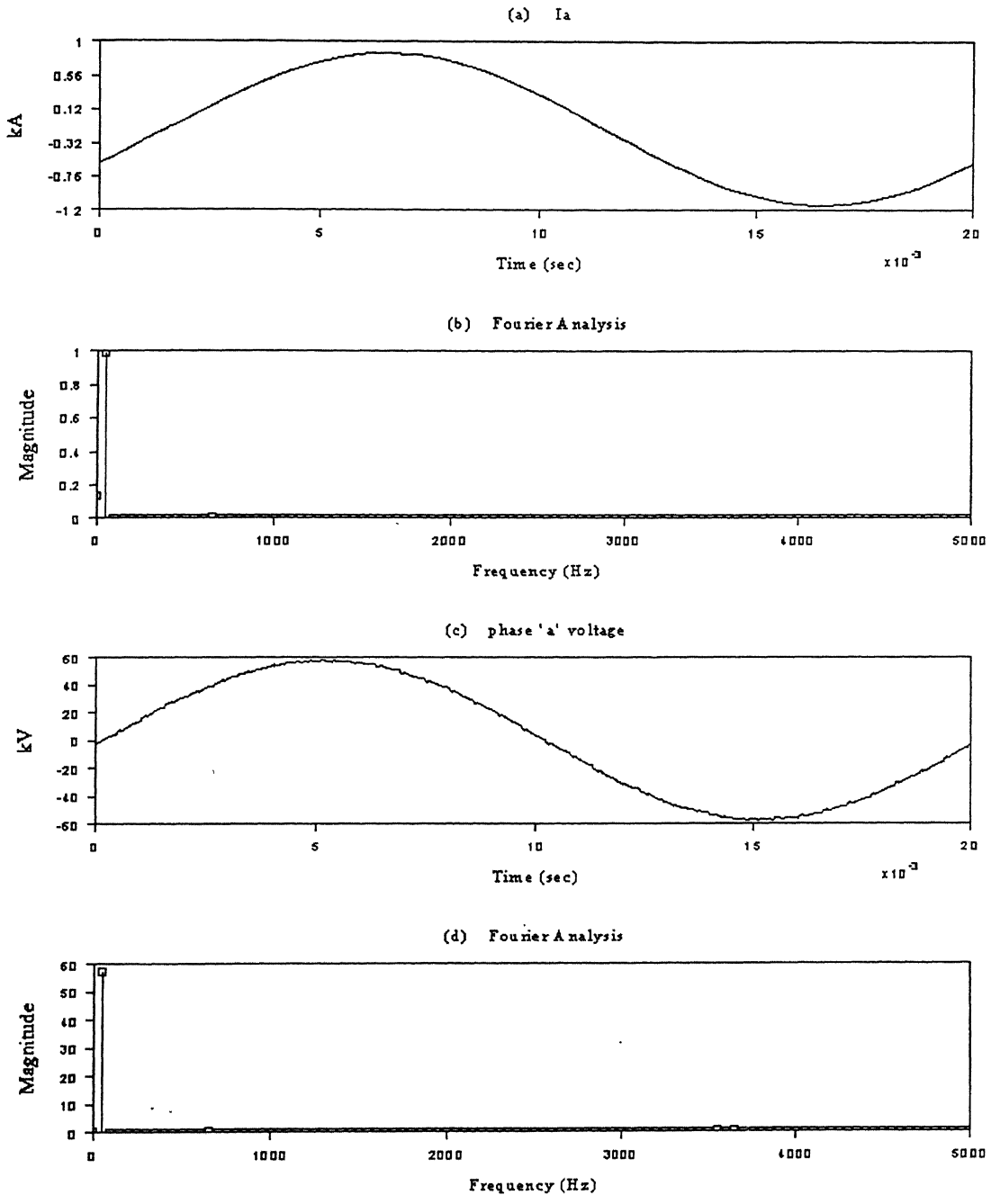

Figure 2.15: Harmonic spectra for a two terminal DC link

Chapter 3

MULTI-PWM VOLTAGE SOURCE CONVERTER BASED HVDC LINK

It was demonstrated in the last chapter that although it is theoretically possible to operate a single-PWM HVDC link with high switching frequency, but practically it is not possible to do so because of limitation of the devices to switch at high frequency at high power levels. To achieve the objective of acceptable harmonic spectrum of the converters at high power levels, multi-PWM configuration of voltage source converters has been reported in the literature. In this chapter, feasibility of operating a HVDC link with multi-PWM VSC at both the sides is investigated in detail.

3.1 Multi-bridge PWM VSC

To improve the harmonic spectra of the output current, the idea of combining the harmonic neutralization effect of a multi bridge configuration and that of a PWM converter has been proposed in the literature. In this scheme, a number of PWM converter bridges are connected in union to form a multi bridge PWM converter. In [9], it has been shown that if 'n' PWM converter modules are connected with their individual triangular carrier wave suitably phase shifted, the overall carrier wave frequency of the complete multi bridge PWM converter becomes nf_c, where f_c is the carrier wave frequency of an individual PWM converter. Thus by this method, the effective frequency ratio K_c (i.e. ratio of the carrier wave frequency to the reference wave frequency) increases 'n' times and as a result, the harmonic content of the output voltage of the multi-bridge PWM converter will be greatly reduced, while ensuring that the switching frequency of an individual bridge does not cross the practical limit of 500Hz.

The schematic diagram of a converter station using a parallel connected multi PWM converter connected to an AC system is shown in Fig. 3.1. In this work, the carrier frequency of each of the four converter blocks has been chosen as 450 Hz, while the modulation frequency (i.e. frequency of the reference wave) is 50 Hz. The carrier wave of the second inverter lags that of the first by 90° in its own frequency (i.e. 10° on the basis of fundamental frequency). Similarly, the carrier wave of the third converter lags that of the second one by 90° and so on.

The effective carrier frequency of the multi PWM converter is then 4 x 450 = 1800Hz [9], i.e. 36 times the fundamental frequency giving K_c = 36. Hence, the harmonic content of the output voltage of the configuration will be drastically reduced. From Fig. 3.1 it can be observed that the outputs of the individual bridge are connected through interphase reactances (X_i). These reactances are required to prevent sudden upsurge of the current in each phase. This upsurge may occur when the devices in the same phase are switched 'ON' directly across the DC capacitor.

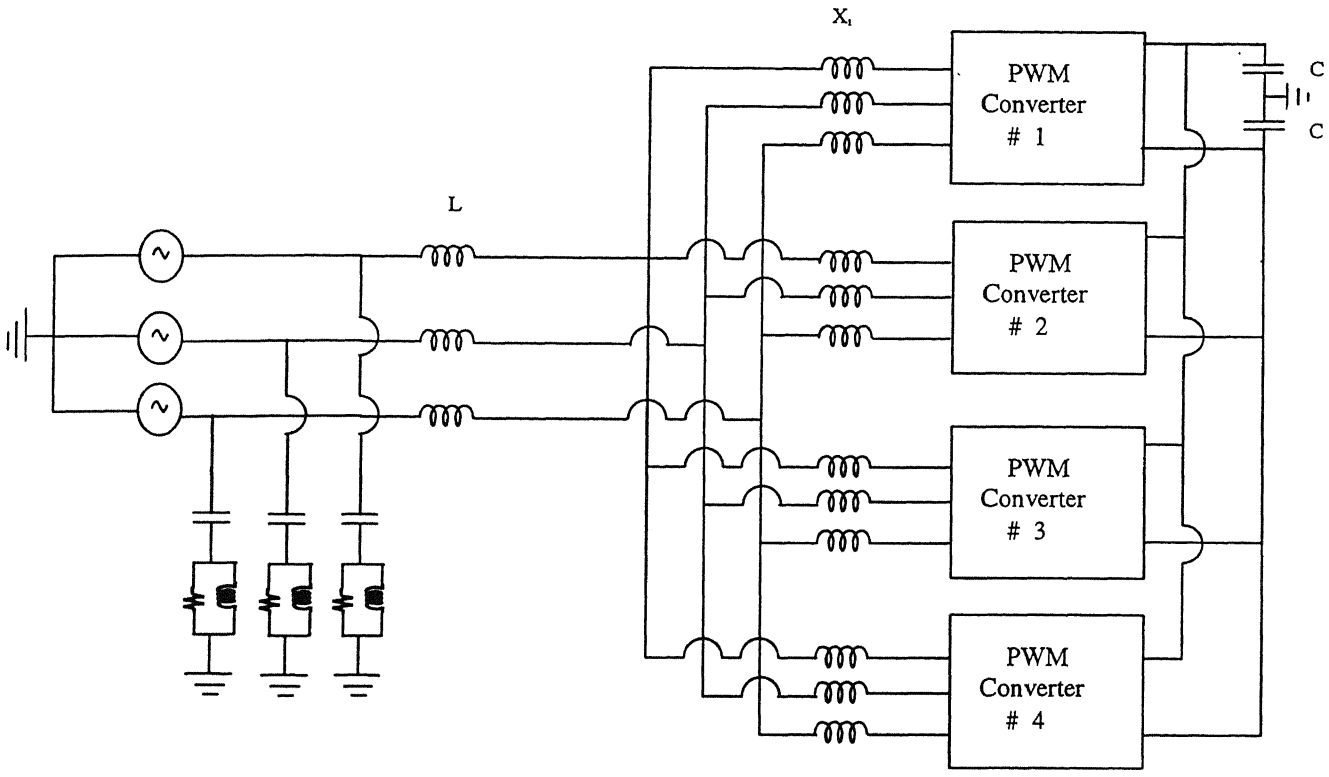

Figure 3.1: Schematic diagram of a single converter station

As the harmonic content of the output voltage of a multi-PWM VSC is expected to be quite low while limiting the switching frequency of individual PWM converter within the practical limit of 500 Hz., the feasibility of using a multi-PWM VSC based HVDC link has been investigated in this work. It is expected that a multi-PWM VSC based HVDC link may offer a practical solution to the problem of high power transfer while maintaining an acceptable harmonic content in the system. In the next section, such a scheme is described in detail.

3.2 Multi PWM VSC based HVDC scheme

A schematic diagram of a multi-PWM VSC based HVDC scheme is shown in Fig. 3.2. The value of the DC capacitor has been chosen as 500 μF, which is higher than the value decided upon in the last chapter. This is due to the fact that in a parallel connected multi-PWM VSC, the effective switching frequency of the DC capacitor is 450 Hz. (as each converter is switching at a frequency of 450 Hz.). Hence, to reduce the harmonics on the DC side the value of the DC capacitor needs to be increased. However, the value of the converter reactor for each converter has been chosen as 0.1 H, which is lower than the designed value in previous chapter. This is due to the fact that the harmonic content of a multi-PWM VSC is considerably lower than that of a single-PWM VSC. Thus, for same amount of harmonic component in the line current in both the cases, the value of converter reactor with multi-PWM VSC is less than that with single-PWM VSC. The two converters at each side (rectifier and inverter) are identical in nature. These two stations are connected through a HVDC link and the parameters of the link are identically the same as those have been used in the previous chapter. The same type of filters as used in the previous chapter has also been used in this system. However, as the harmonic contents are different in this case are different than in the case with single PWM VSC, the parameters of the filters are also not identical to those used in the previous chapter. The filter parameters used for this case are as follows : quality factor = 10.0, and cutoff frequency = 1550 Hz. In this study, the rectifier side DC voltage is being maintained at 160 kV and the inverter side AC power is maintained at 40 MW. To achiever this, two PI controllers, as shown in Figs. 2.12 and 2.13 respectively, are being used in the rectifier and inverter sides. The proportional gain (K_p) and the integral gain (K_i) at the rectifier side have been chosen as 0.0 and 14.0 respectively. Similarly, at the inverter side, the proportional gain (K_p) and the integral gain (K_i) have been chosen as 0.0 and 2.5 respectively.

The steady state performance of the link is shown in Fig. 3.3. The figure shows the traces of response of the rectifier side PI controller (part a), rectifier side DC voltage (part b), inverter side DC voltage (part c), response of the inverter side PI controller (part d), and inverter side active power (part e). It is observed from this figure that the proposed controllers are able to maintain the rectifier side DC voltage and the inverter side active power to their respective reference values faithfully. To analyze the harmonic spectrum in various quantities in the system, traces of one cycle of `a'-phase line current at the rectifier side and one cycle of `a'-phase

voltage at the rectifier side at point `a' (shown in Fig. 3.2), at steady state condition, are shown in Fig. 3.4. The harmonic spectrum of these two signals obtained by Fourier analysis are also shown in this figure. It is observed from this figure that there is very little amount of harmonics in the system. This clearly establishes the fact that the harmonic content of the multi-PWM VSC based HVDC system is quite acceptable while maintaining the switching frequency of individual converters within the practical limit of 500 Hz.

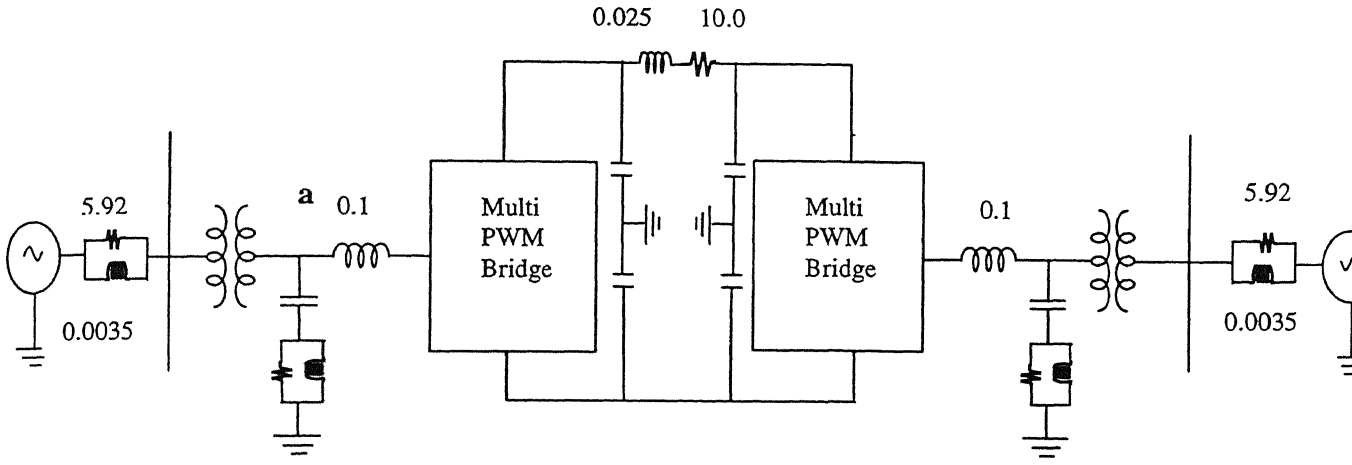

Figure 3.2: Schematic Diagram of a two terminal DC link using multi-PWM bridge.

To investigate the capability of the controllers to accommodate variable power demand at the inverter side, simulation studies with step changes in the power demand at the inverter side have been carried out. In this study, the power demand at the inverter side has been reduced in one step from 40 MW to 30 MW at t = 0.2 sec and subsequently it has been increased from 30 MW to 50 MW in one step at t = 1.0 sec. And finally, it has been brought down to 40 MW from 50 MW at t = 1.9 Sec. The results are shown in Fig. 3.5. Again, in this figure also, the traces of response of the rectifier side PI controller (part a), rectifier side DC voltage (part b), inverter side DC voltage (part c), response of the inverter side PI controller (part d), and inverter side active power (part e) are shown. From this figure it is clearly observed that the proposed controllers are able to follow the step changes in the power demand at the inverter side faithfully.

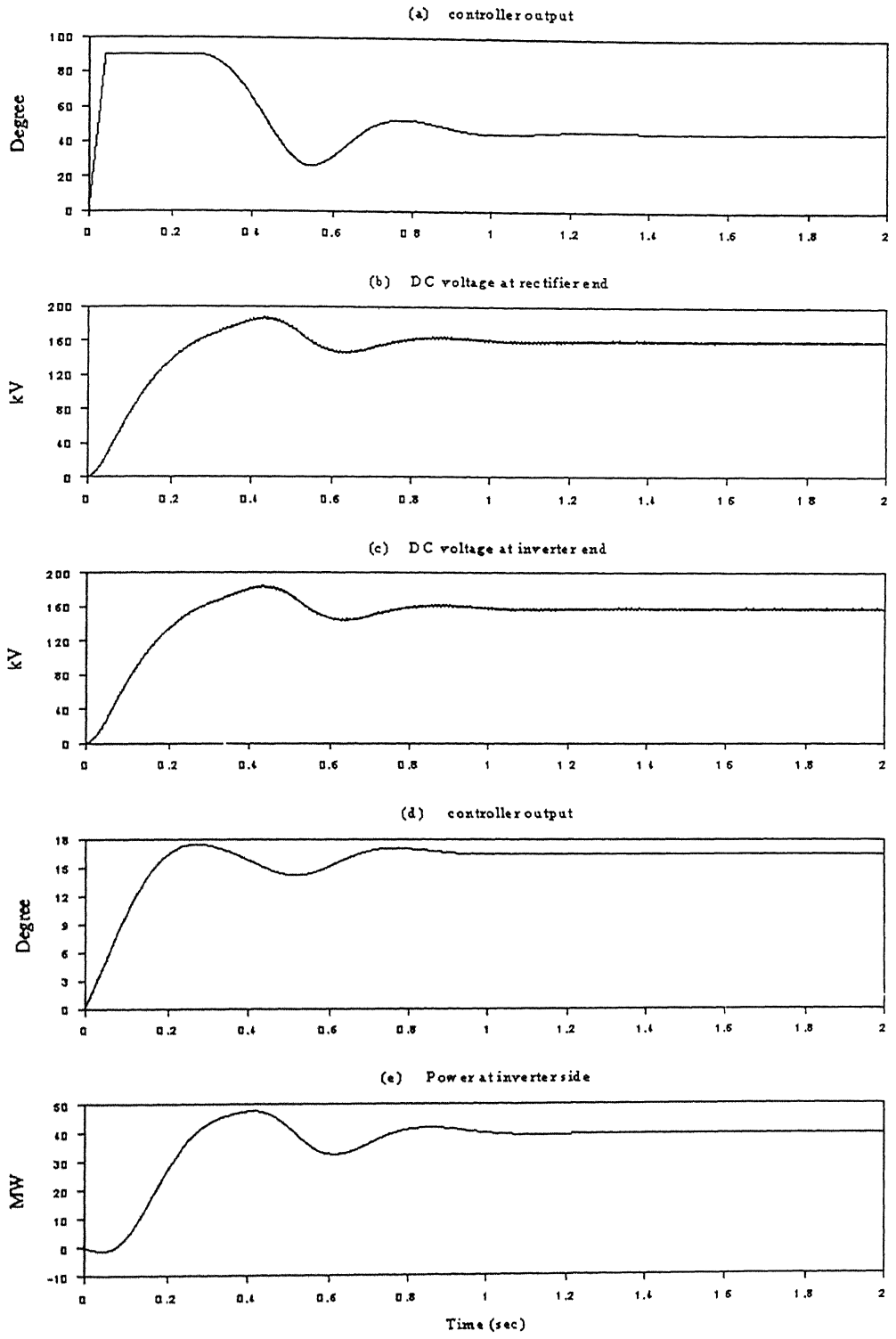

Figure 3.3: Steady state performance of HVDC link

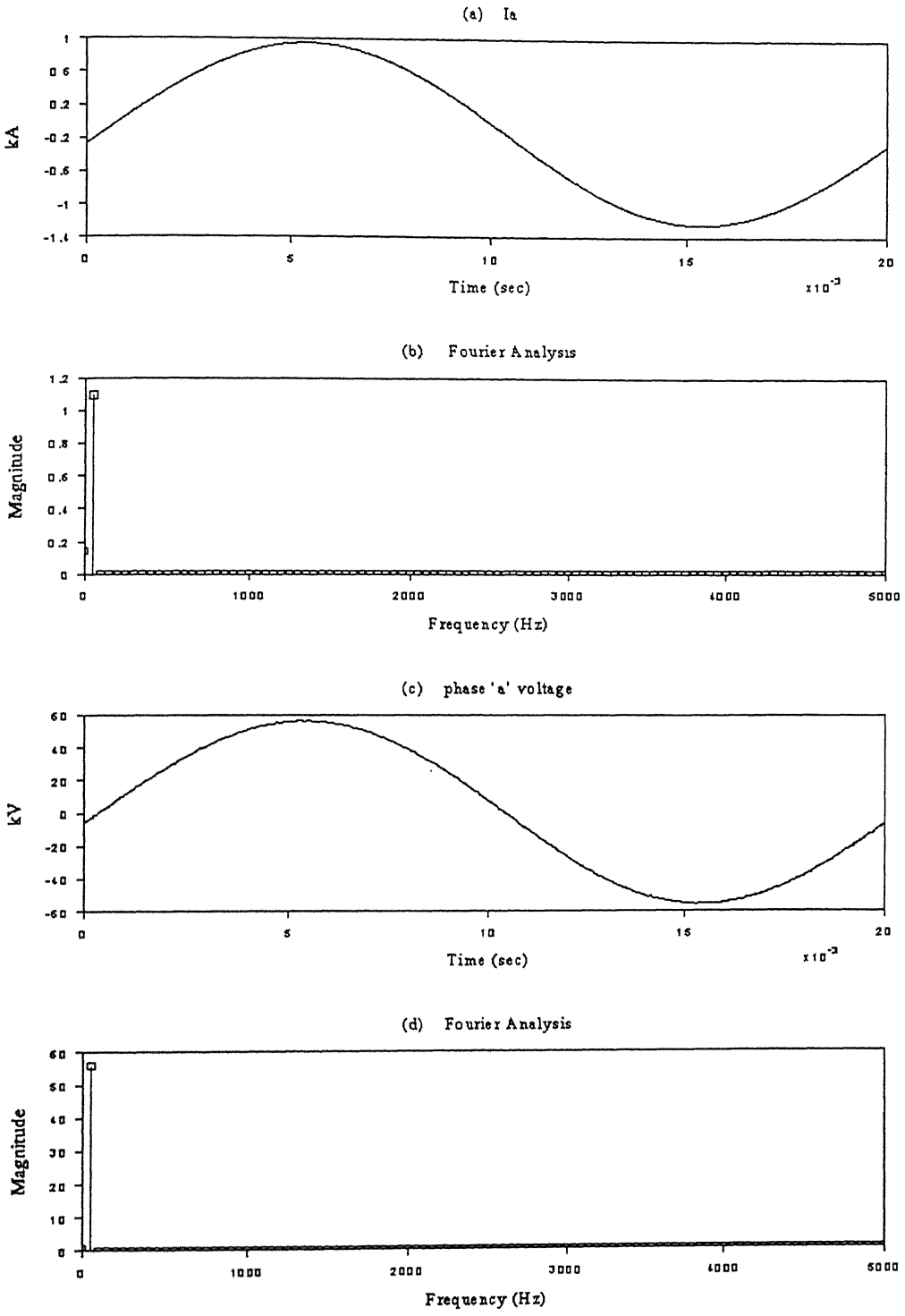

Figure 3.4: Harmonic Spectra of the HVDC link under steady state

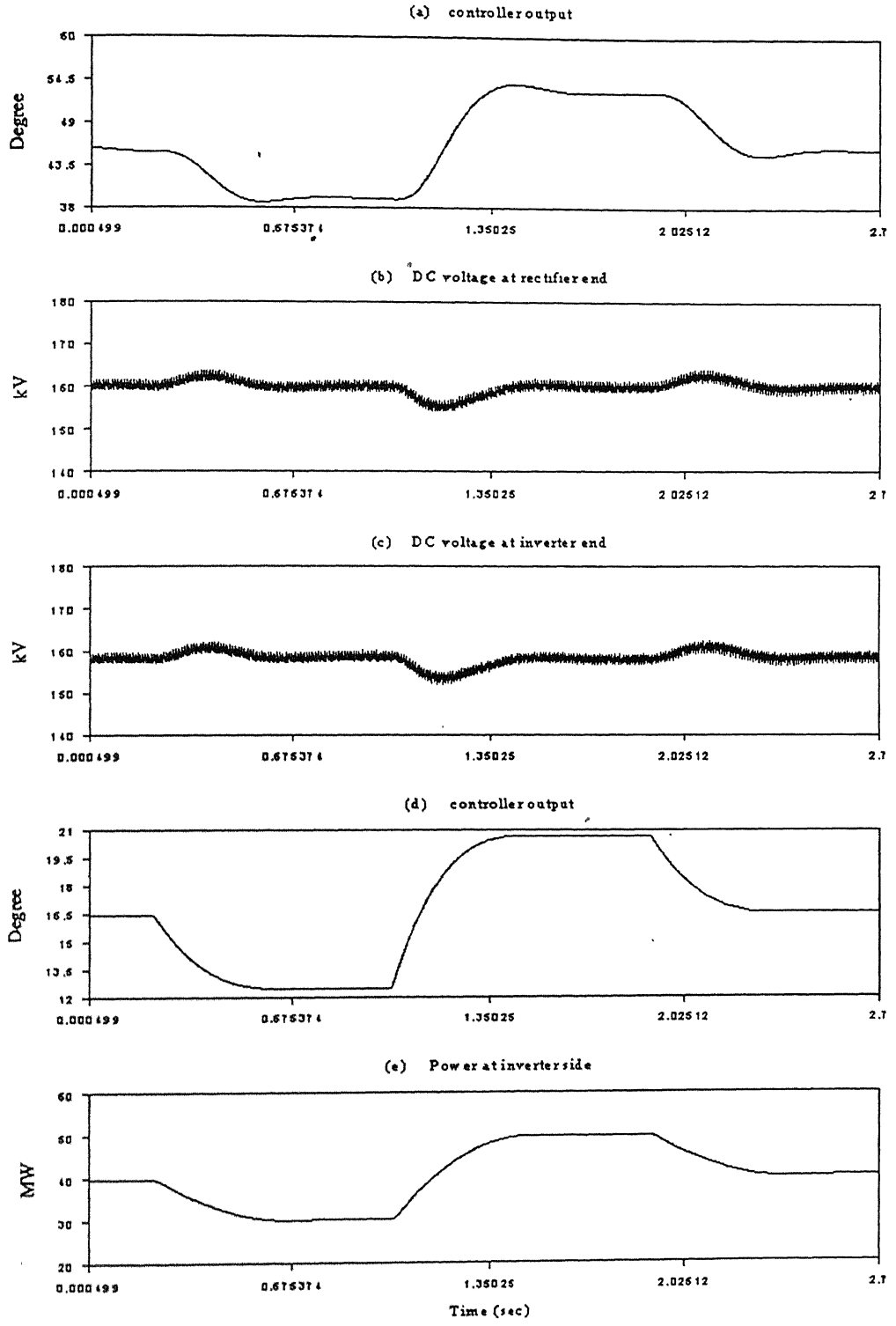

Figure 3.5 : Step change in power demand at inverter side

To investigate the effectiveness of the proposed controllers under transient conditions, simulation studies have been carried out for different fault conditions at both the AC sides of the rectifier and the inverter stations. For these transient studies, the rectifier side DC capacitor voltage has been fixed at 160 kV (as in the previous case). However, to test the performance of the controllers at more stressed operating condition, the inverter side steady state power demand has been increased to 50 MW. The different faults, which have been considered in this work, are as follows :

a) 10 cycle, single line-to-ground (1LG) fault.

b) 5 cycle, line-to-line (LL) fault.

c) 5 cycle, line-to-line-to-ground (LLG) fault.

d) 5 cycle, three-line-to-ground (3LG) fault.

Hence, in total, eight different fault cases have been considered. In each case, the fault has been applied at t = 0.2 sec. Fig. 3.6 shows the simulation results for a 3LG fault at the AC side of the rectifier station. From the plots it can be seen that the system is able to withstand the transient conditions through fast dynamic control action. It is to be noted that Fig. 3.6(a) shows the trace of the output of the rectifier side PI controller while Fig. 3.6(d) shows the trace of the output of the inverter side PI controller. When the fault occurs, the voltage and the power on the AC side reduce. Due to this, the DC voltages at both rectifier and inverter side also decrease. To maintain the voltage across the DC capacitor at the rectifier side constant, the controller on the rectifier side increases the angle (δ) between the AC side voltage and the voltage generated by the converter to increase the power flow for charging the capacitor, which starts increasing the DC capacitor voltage. In this process, the output of the rectifier side PI controller hits the upper limit of 90° and remains at that position for some period. Because of the drop of voltage at the inverter side, active power on the AC side of the inverter station also decreases. To maintain this power at the reference value, the controller on the inverter side increases the angle between the AC side voltage and the voltage generated by the converter. When the DC voltage and the active power increase beyond their respective set points, the controllers decrease the angles (δ), and this trend continues till the system comes back to the pre-fault steady state condition. The pre-fault steady state is reached within 2.0 seconds after the commencement of the fault. The simulation results

for LLG, LL and LG faults are shown in Figs. 3.7, 3.8 and 3.9 respectively. These faults are less severe compared to the 3LG fault and hence, as observed from these three figures, they are also successfully controlled by the proposed controllers. The variation of different quantities in Figs. 3.7, 3.8 and 3.9 are quite similar to those in Fig. 3.6 and hence the explanations for these variations are not repeated below.

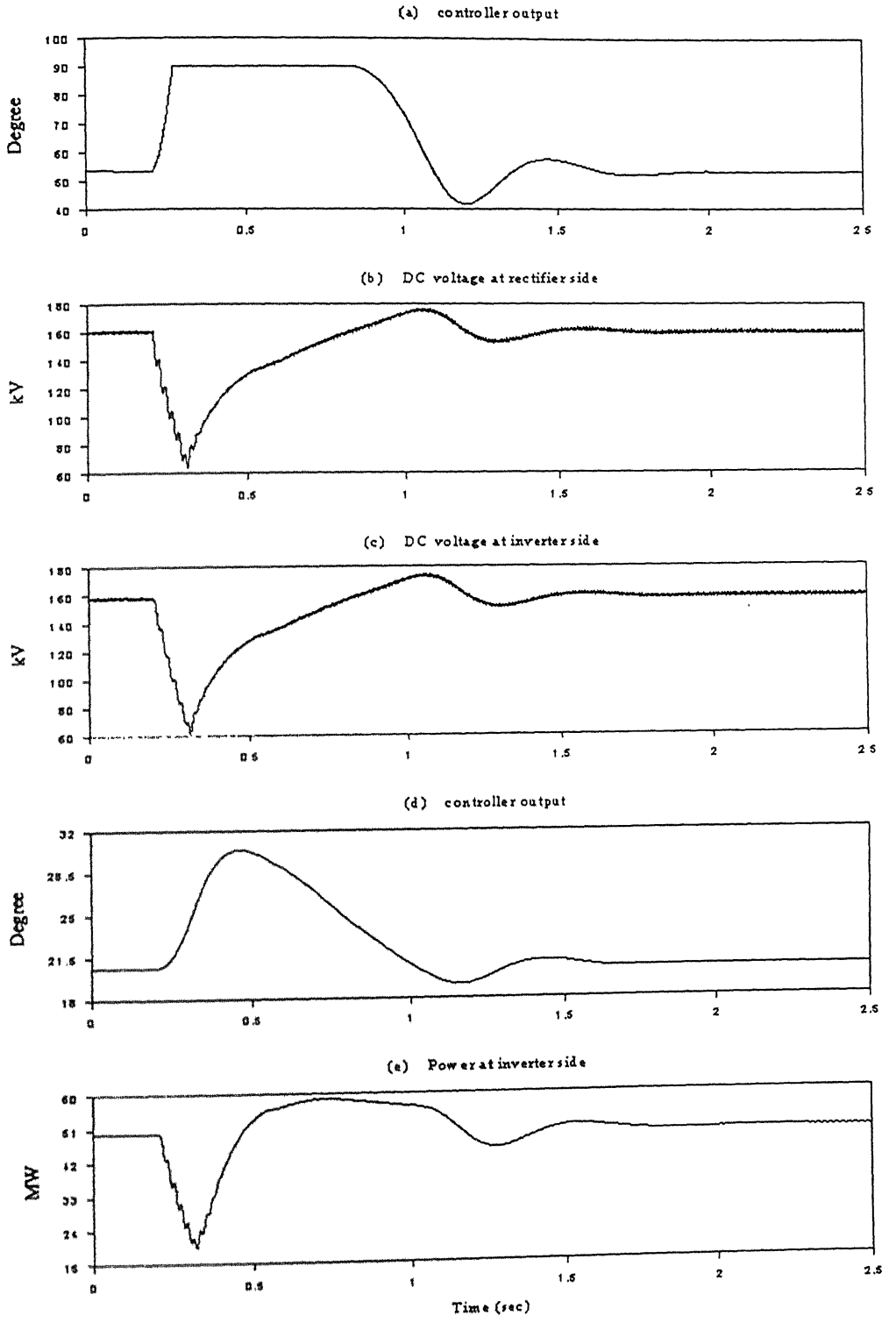

Figure 3.6 : Simulation results for 3LG fault on the AC side of rectifier station.

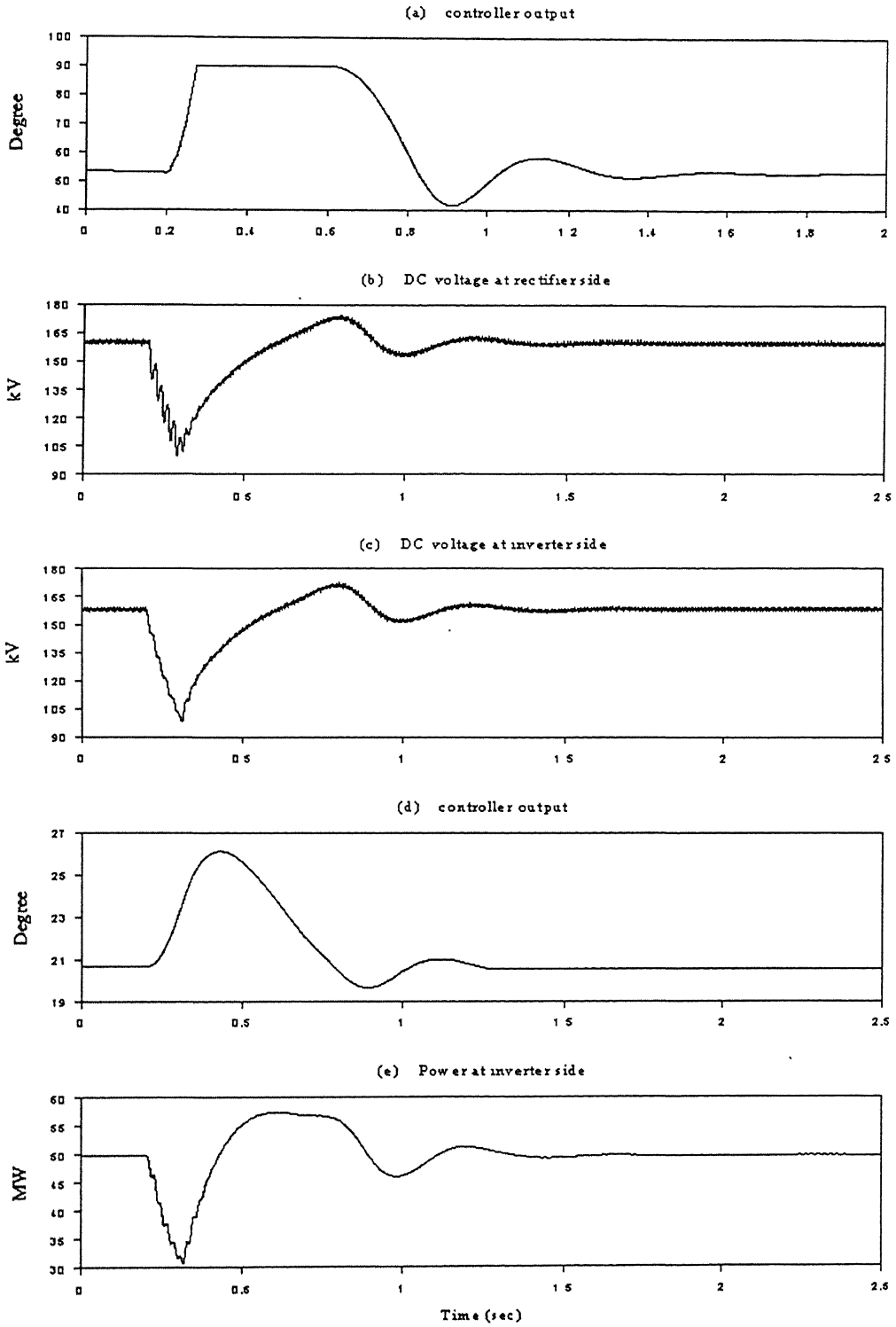

Figure 3.7: Simulation results for LLG fault on the AC side of the rectifier station.

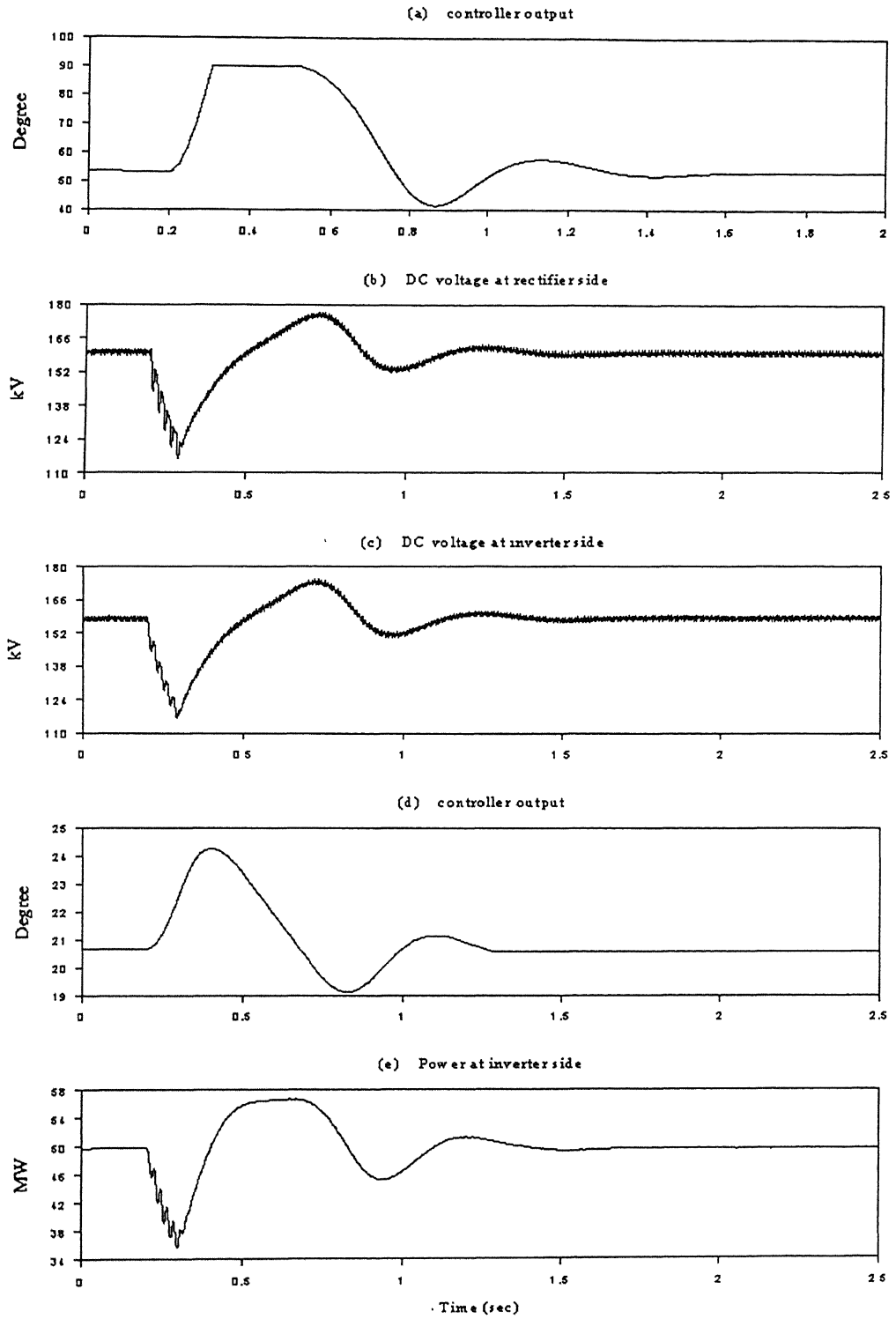

Figure 3.8: Simulation results for LL fault on the AC side of rectifier station.

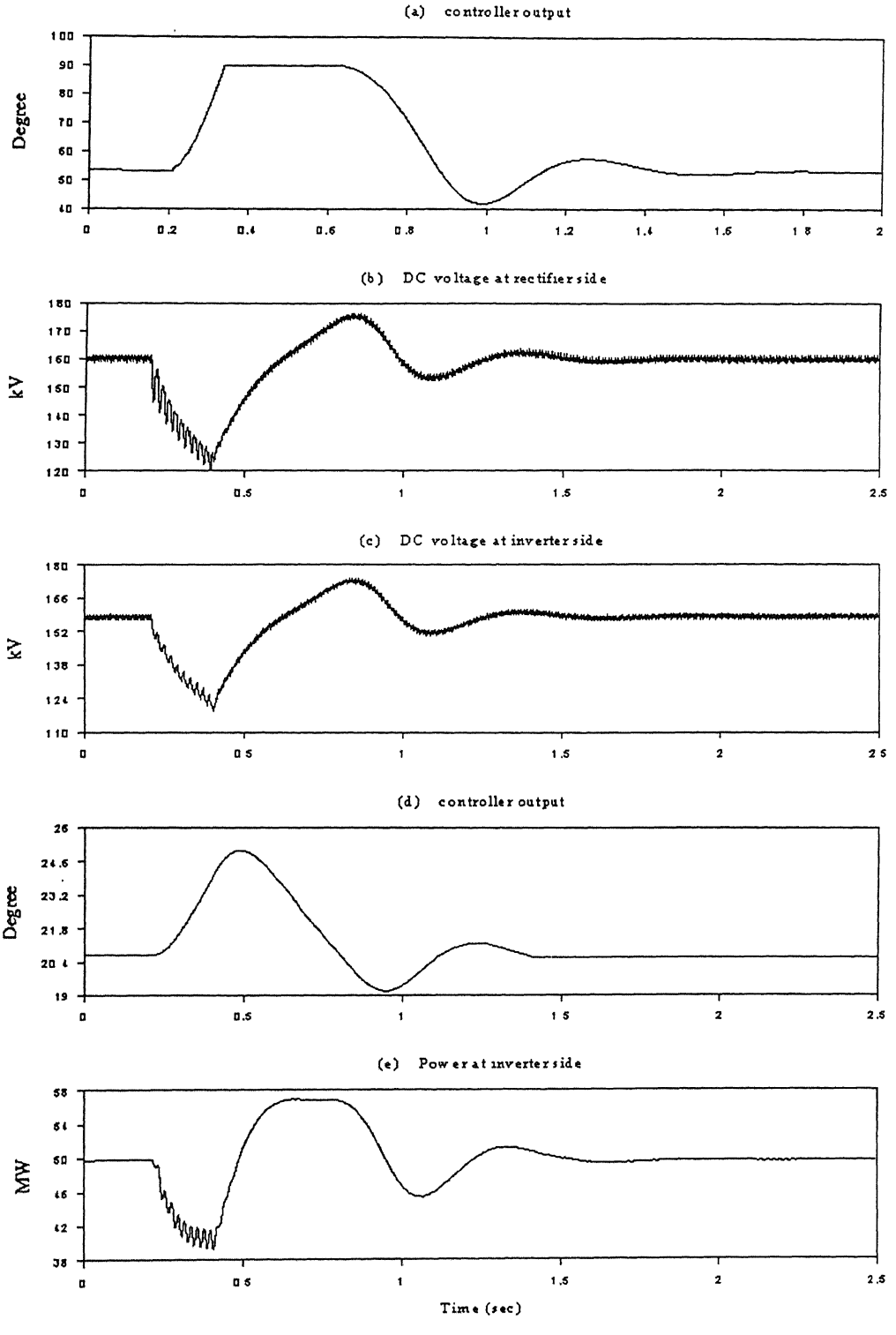

Figure 3.9 : Simulation results for LG fault on AC side of rectifier station.

The simulation results for a 3LG fault at the AC side of the inverter station are shown in Fig. 3.10. As the fault is applied, the active power at the AC side of the inverter decreases. Thus, at the instant of the fault application, power extracted from the rectifier side DC capacitor decreases, whereas, the power supplied to it from the rectifier AC side remains more or less constant. Hence, the voltage of the rectifier side DC capacitor starts increasing. Consequently, the PI controller at the inverter side increases the angle (δ) to bring back the inverter side active power to the set value. On the other hand, the PI controller at the rectifier side decreases the angle (δ) initially to maintain the voltage of the DC capacitor at the reference value, but subsequently, it also increases the angle to meet the requirement of power of the inverter side. The system reaches the pre-fault steady state within 2.5 sec. after the commencement of the fault. The results for LLG, LL and LG faults at the AC side of the inverter station are shown in Figs. 3.11, 3.12 and 3.13 respectively. As the variations of different quantities in these three figures are quite similar to those of in Fig. 3.10 , these are not explained again.

The above results clearly demonstrate the technical feasibility of transmission of power between two AC systems over a multi-PWM VSC based HVDC system. However, a major advantage of VSC based HVDC scheme over line-commutated converter based HVDC scheme is the apparent capability of the former to supply a passive load, which is not otherwise possible by the later. In the next chapter, the technical feasibility of supplying a passive load by multi-PWM VSC based HVDC scheme is investigated in detail.

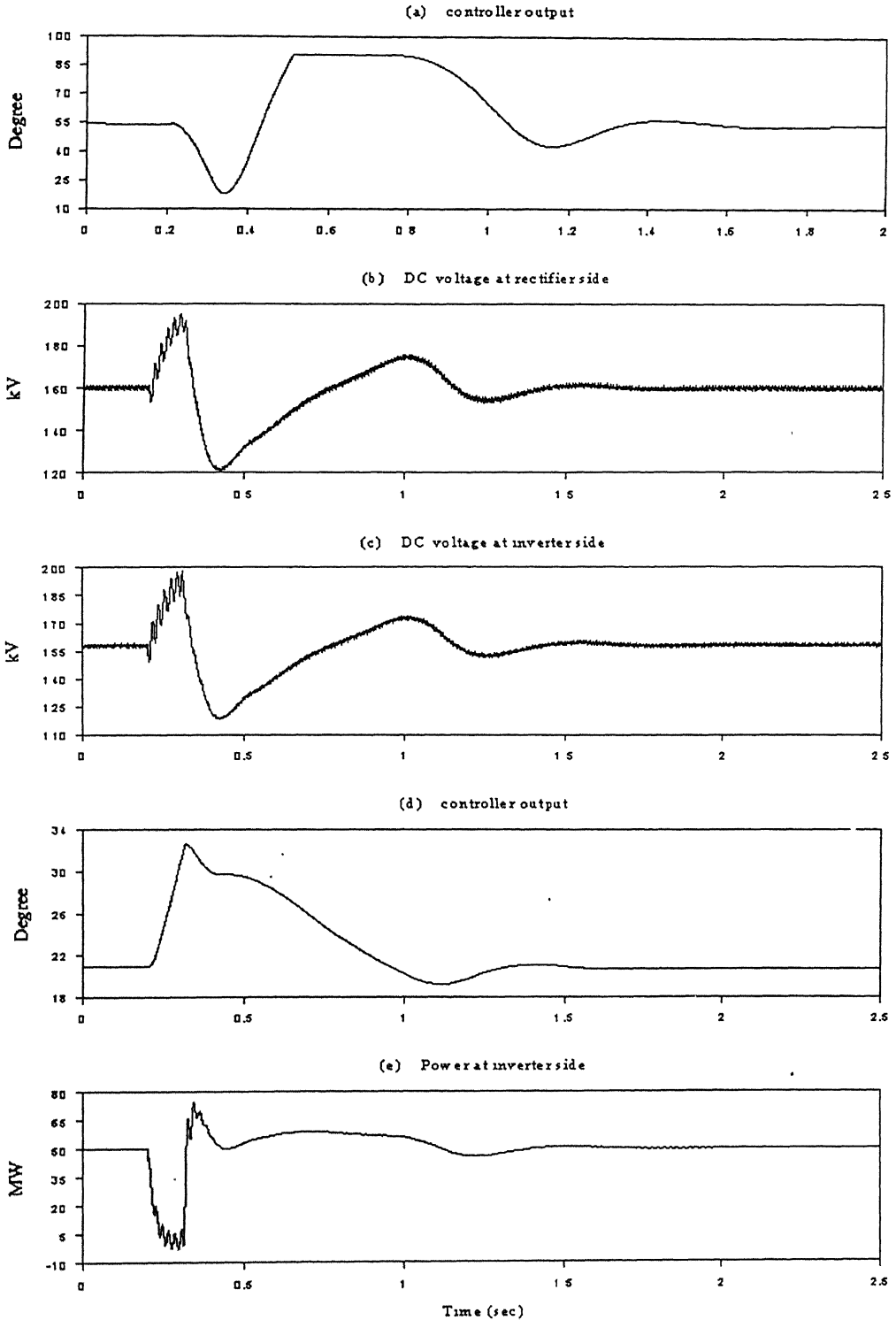

Figure 3.10 : Simulation results for 3LG fault on the AC side of inverter station.

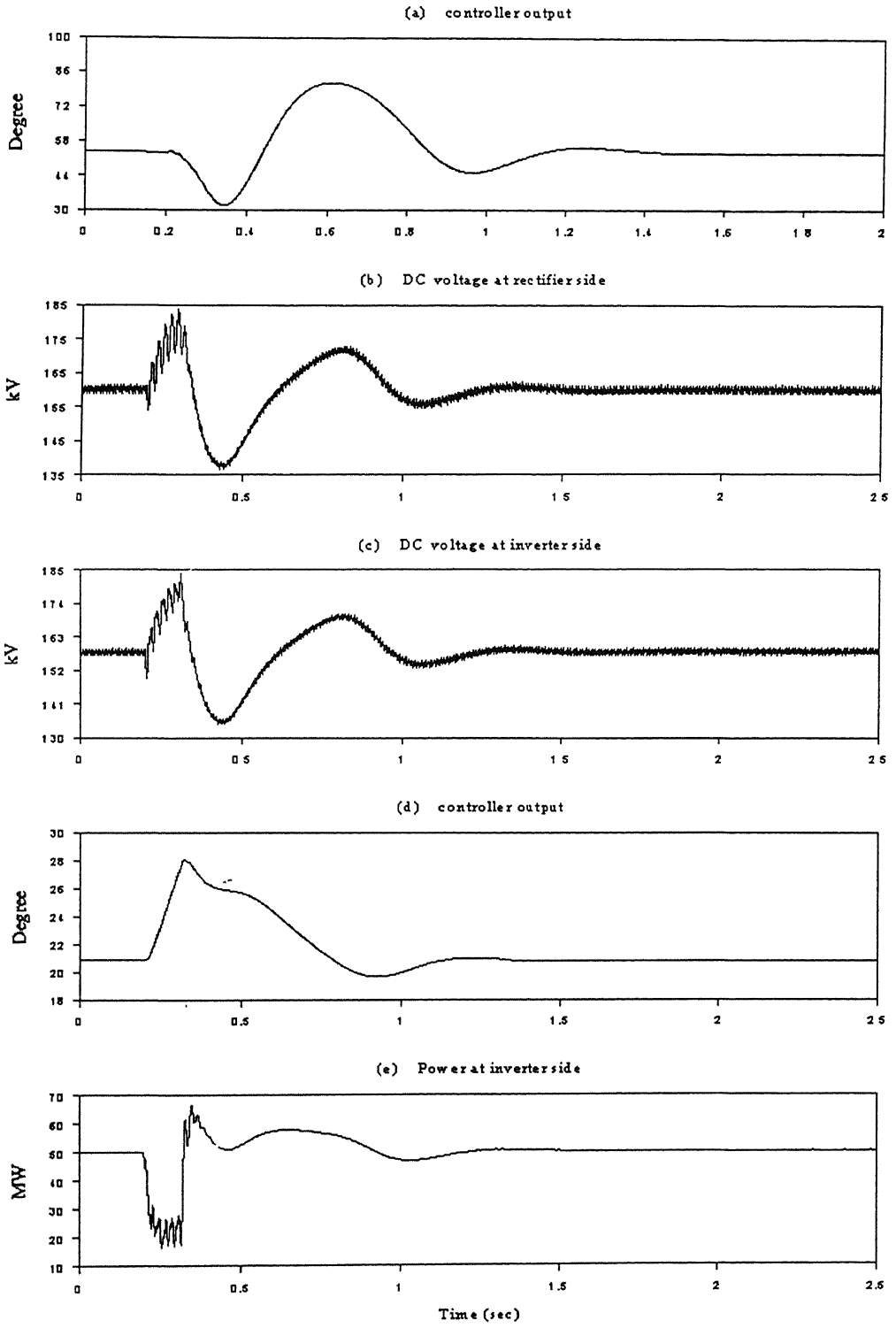

Figure 3.11 : Simulation results for LLG fault on the AC side of inverter station.

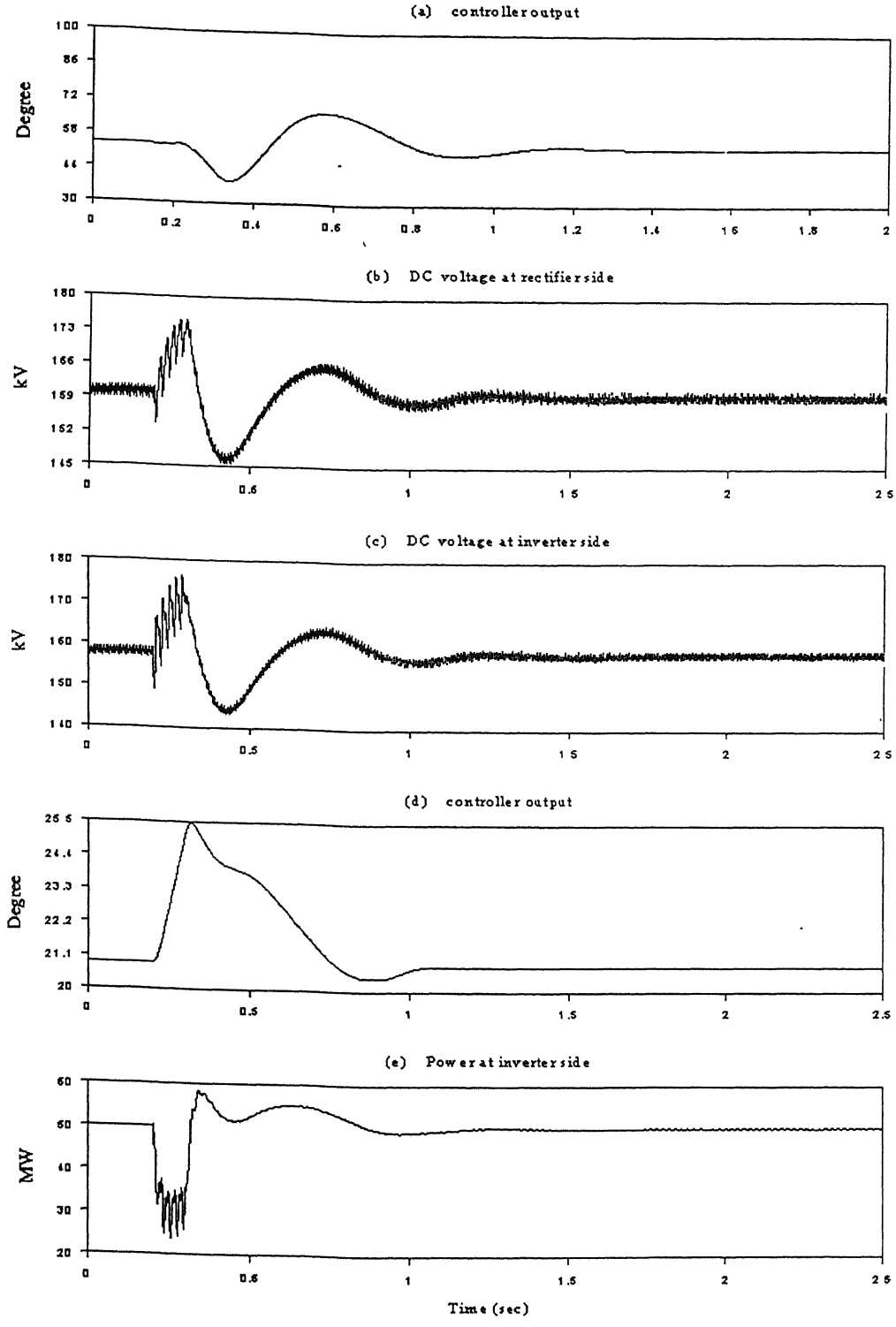

Figure 3.12: Simulation results for LL fault on the AC side of inverter station.

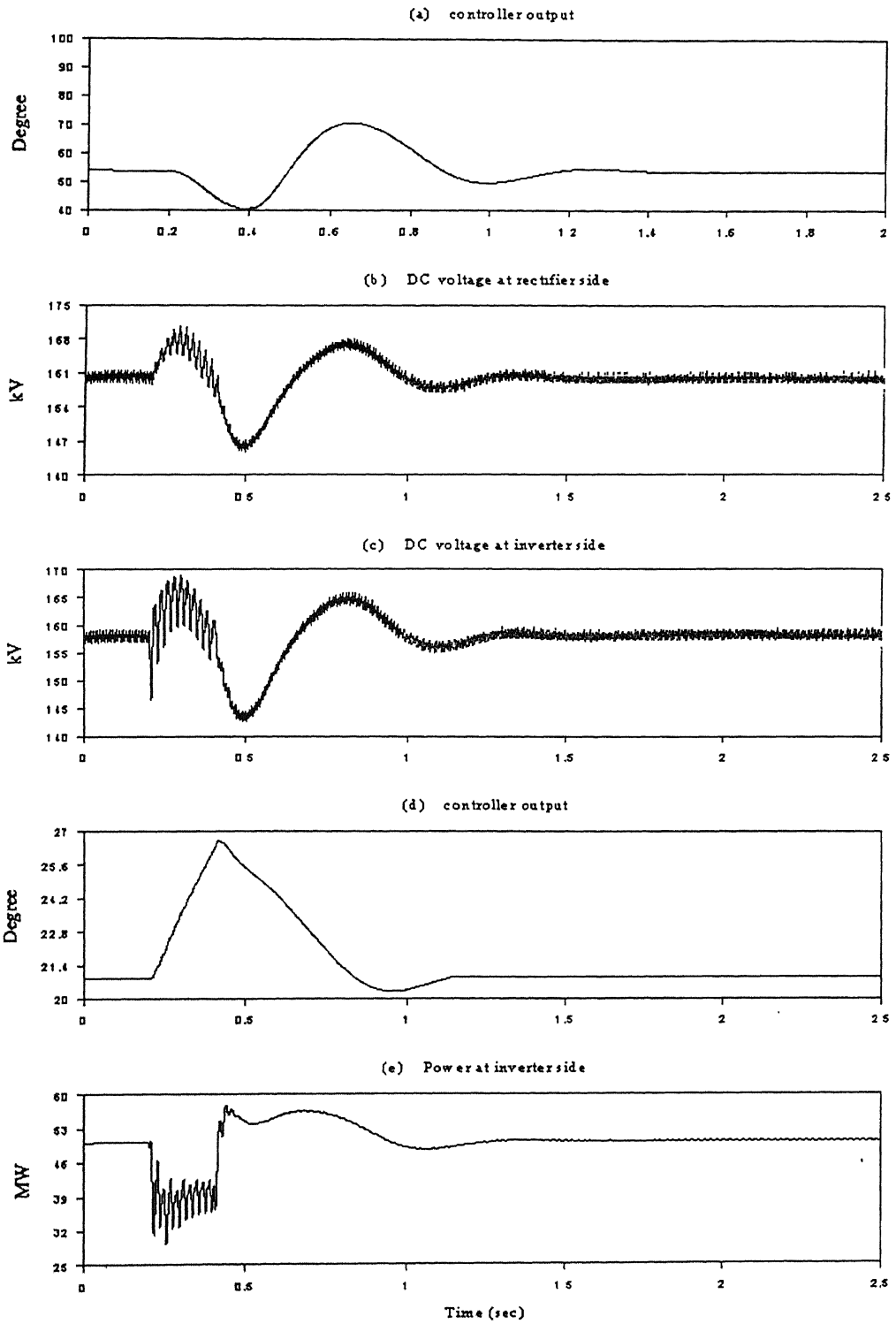

Figure 3.13: Simulation results for LG fault on the AC side of inverter station

Chapter 4

SUPPLYING PASSIVE LOAD BY VSC BASED HVDC LINK

In the last chapter, the technical feasibility of transmission of power between two AC systems over a multi-PWM VSC based HVDC system has been demonstrated. In this chapter, feasibility of supplying passive loads by VSC based HVDC scheme is investigated in detail. Fig. 4.1 shows the schematic diagram of the system considered. Two types of loads have been considered to show that the scheme is able to feed the loads in the steady state as well as under transient conditions. The loads considered are as follows:

- Three-phase, balanced, constant resistive load.
- Three-phase, balanced, variable resistive load.

In the next two sections, these two applications are considered in detail. In the above two cases also, the value of the DC capacitor has been taken as 500 μF.

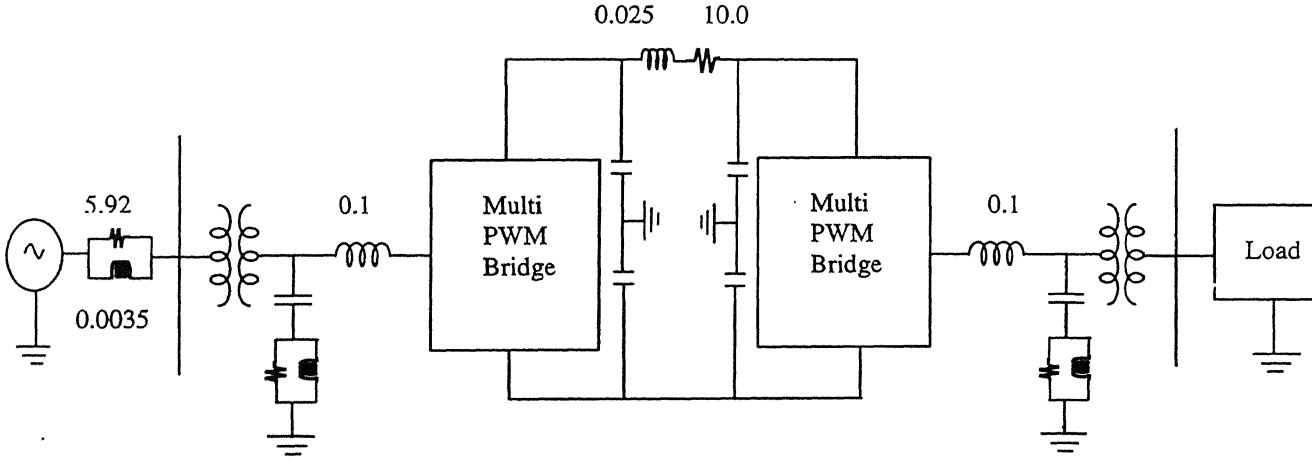

Figure 4.1: Schematic Diagram of a two terminal DC link supplying a load.

4.1 Three-phase balanced constant resistive load

In this case, the load in each phase is represented by a constant resistance. The value of the resistance in each phase has been chosen as 22.0 ohm. In Fig. 4.1, the transformer at each side is rated 100 MVA, 80/33 kV and the resistive load is connected at the 33 kV side. Thus, the resistive load is expected to draw (33*33/22) = 49.5 MW of 3 phase power under nominal voltage condition. For operation of the HVDC system, only one PI controller at the rectifier for controlling the DC capacitor voltage has been employed. The reference voltage setting of the capacitor has been kept at 160 kV as before. The parameters of the PI controller are as follows : K_p = 0.0 and K_i = 20.0. The steady state simulation results are shown in Fig. 4.2. From this figure it is observed that the PI controller is able to maintain the rectifier DC capacitor voltage at the set value. Because of the voltage drop in the system, the voltage at the load bus reduces to 31 kV from the nominal 33 kV. Accordingly, the 3-phase power drawn by the load under this depressed voltage condition also reduces to roughly 45 MW as shown in Fig. 4.2(d). The traces of one cycle of load current and one cycle of `a'-phase load voltage are shown in Fig. 4.3. The results of Fourier analysis of these two quantities are also shown in this figure. From this figure, it is observed that there is very negligible amount of harmonics in the load current and voltage. Thus, multi-PWM VSC based HVDC scheme is quite suitable for supplying quality power to a passive load, which is otherwise not possible by a line-commutated converter based HVDC system.

To investigate the effectiveness of the controller to withstand transient faults, different fault cases as in Chapter 3 have also been studied here. The simulation results for a 5 cycle, 3LG fault at the AC side of the rectifier station are shown in Fig. 4.4. From this figure it is clear that the controller is quite able to withstand this fault and bring the system at pre-fault steady state condition once the fault is removed. Similarly, for a 3LG fault at the AC side of the inverter station, the simulation results are shown in Fig. 4.5. As observed form this figure, the control system is able to withstand this fault also. Different asymmetrical faults, such as LLG, LL and LG faults have also been applied at both ends. For each of these faults, the controller has been able to maintain the stability of the system. The simulation results for these asymmetrical faults are quite similar to those in Fig. 4.4 and Fig 4.5, and hence, these results are not reproduced in this chapter.

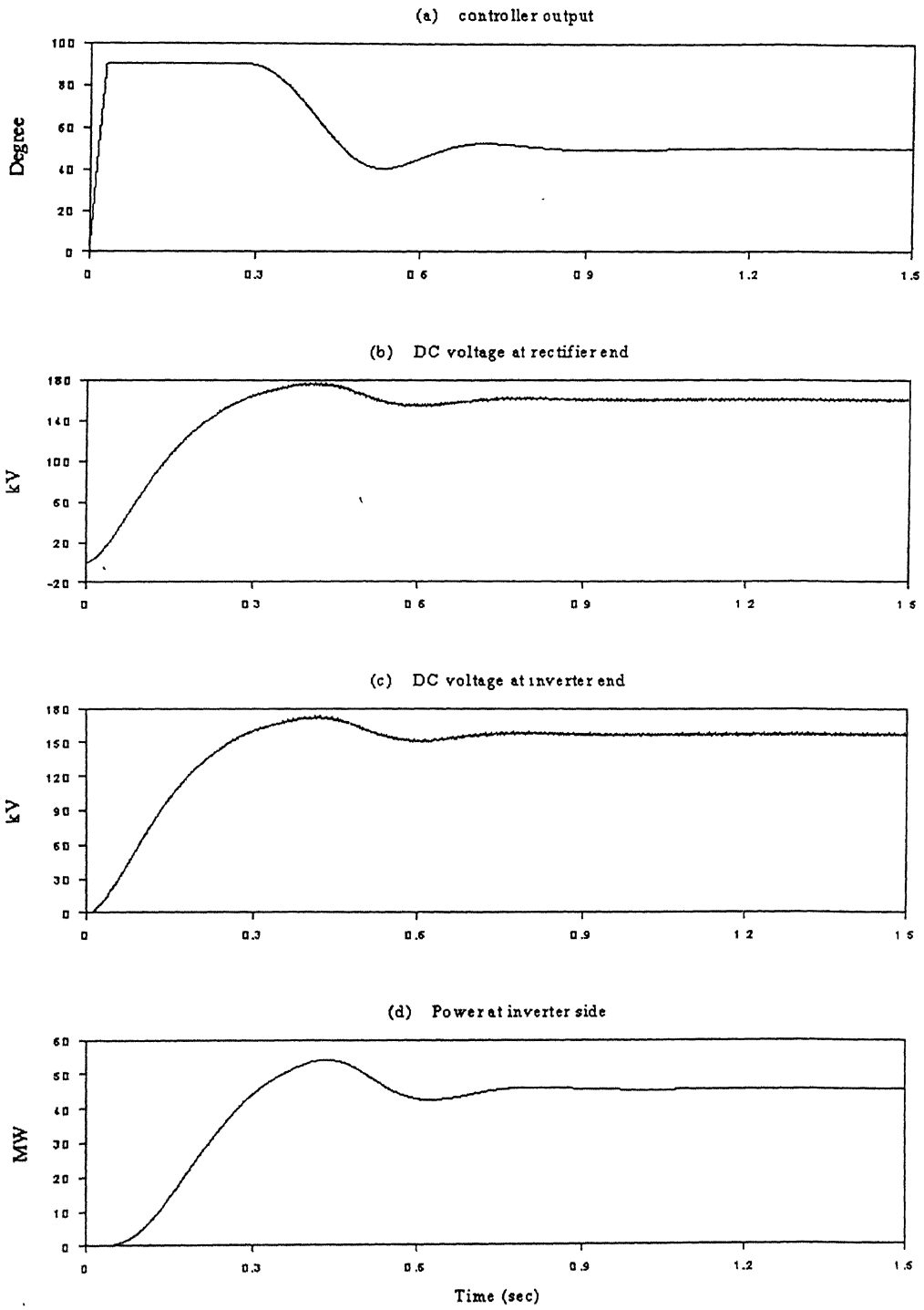

Figure 4.2: Simulation results for Resistive load at steady state.

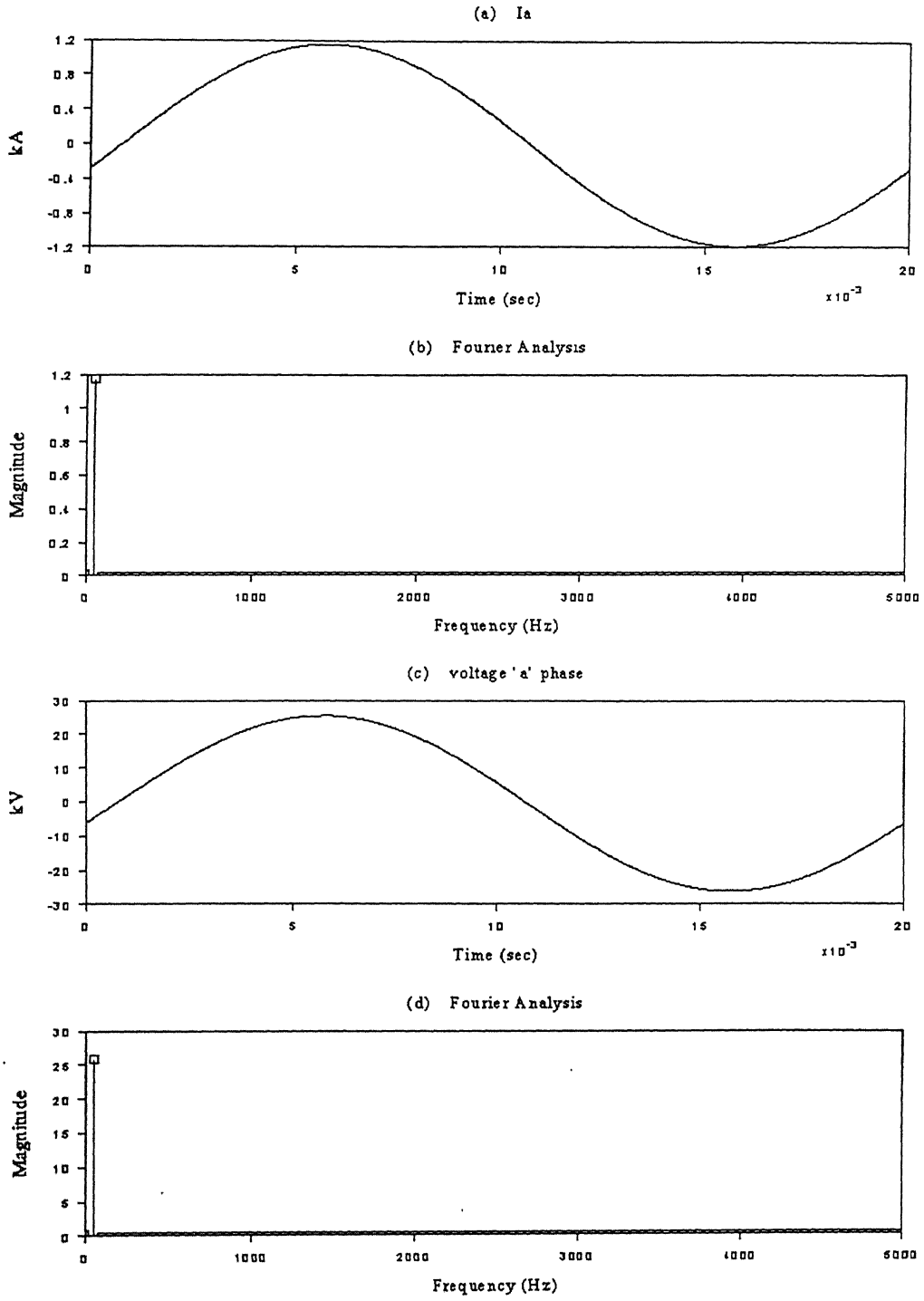

Figure 4.3: Harmonic Spectra of the current and voltage at load end.

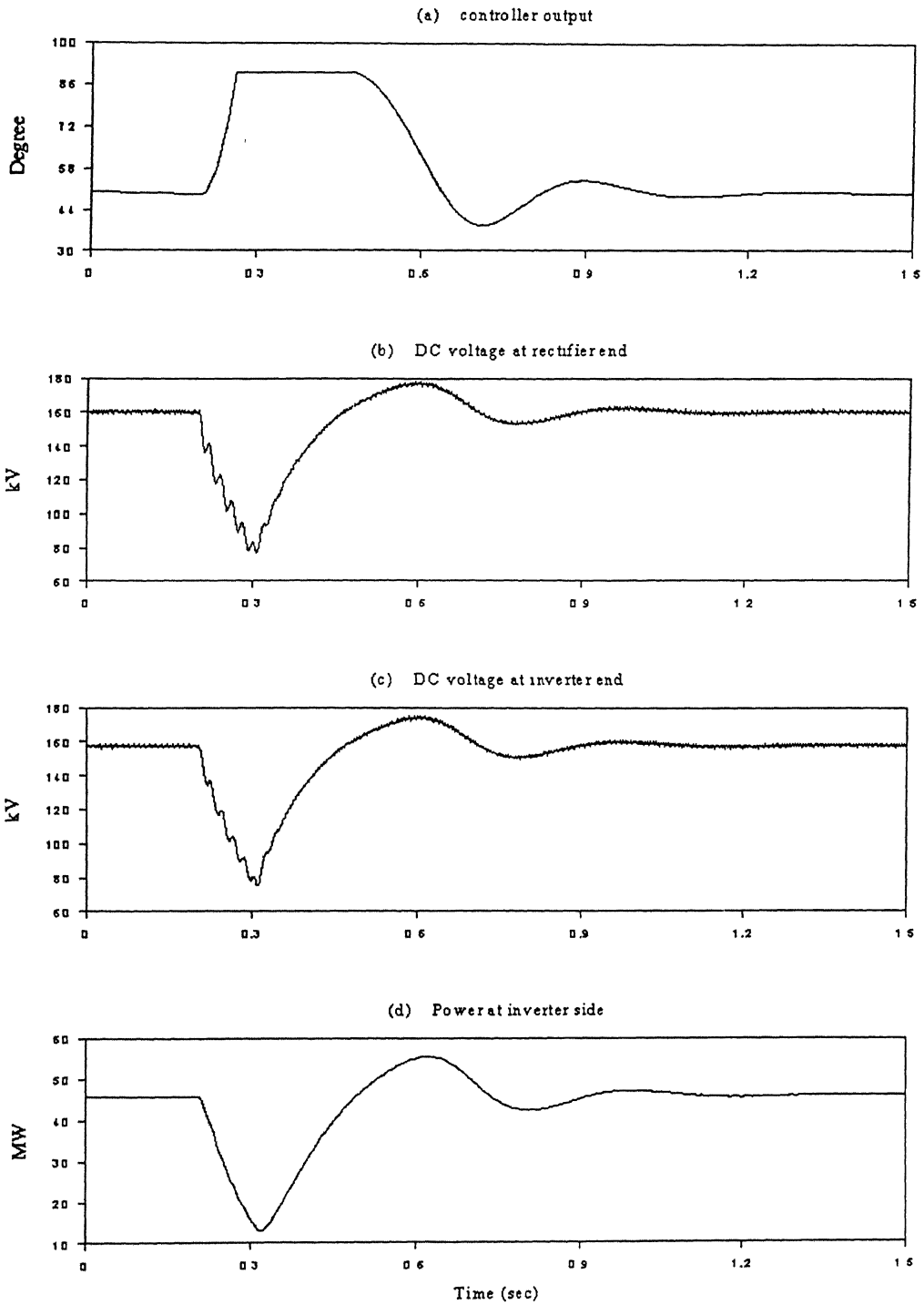

Figure 4.4: Simulation results for the 3LG fault at the AC side of rectifier station

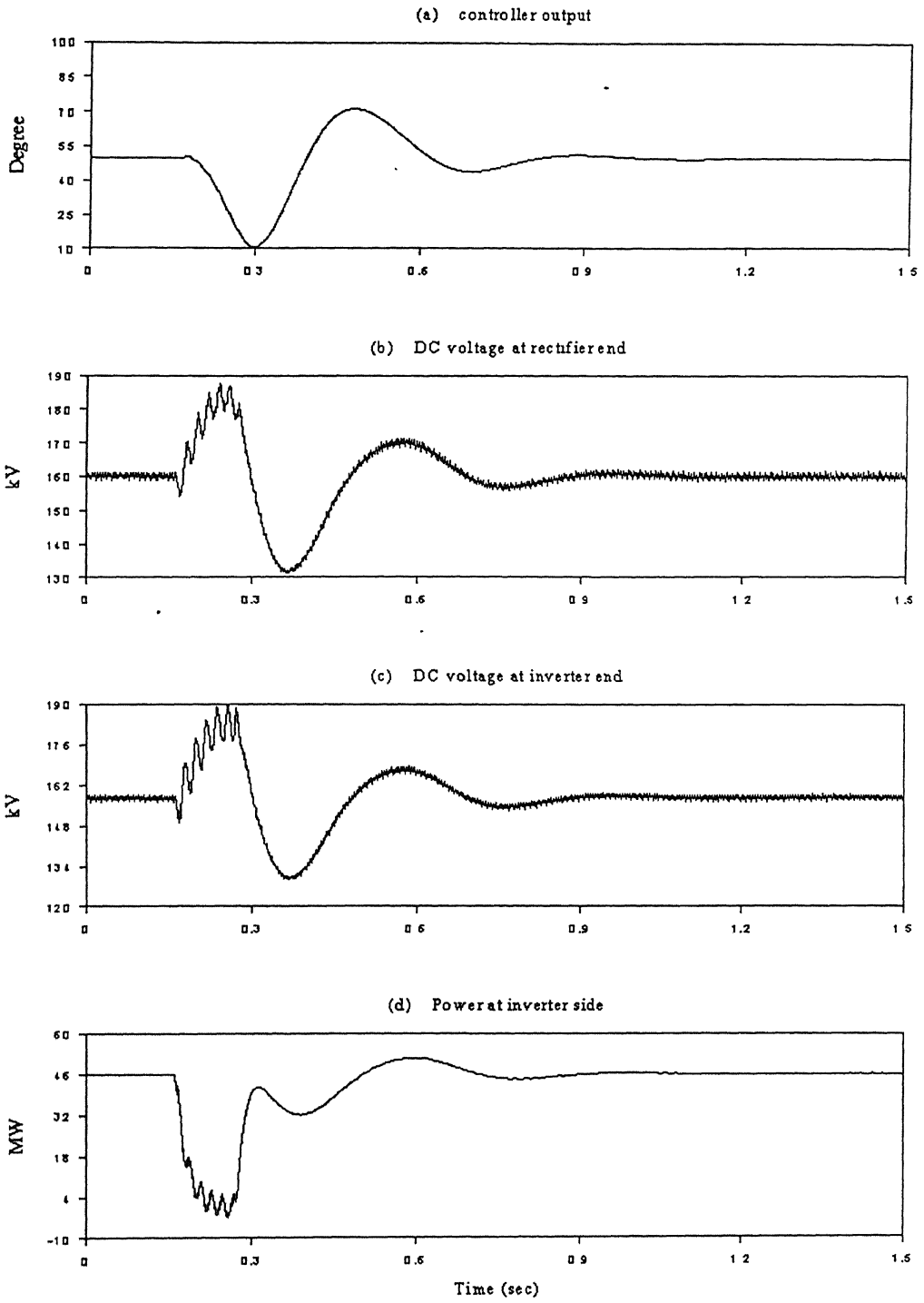

Figure 4.5: Simulation results for 3LG fault at the load end.

4.2 Three-phase balanced variable resistive load

In this case, an investigation has been made to study the capability of VSC based HVDC link for supplying a balanced variable resistive load. The time variation of the resistance of the load has been considered as $R(t) = R_f[1+\sin(2\pi ft)]$. The value of the frequency `f' has been chosen as 10 Hz., and that of R_f has been chosen as 26Ω [12]. Only a PI controller at the rectifier side, as in the last section, has also been used here. The parameters of the controller have been chosen as : $K_p = 0$ and $K_i = 33.33$. The steady state simulation results are shown in Fig. 4.6. From this figure, it is observed that, as the load resistance is varying periodically, the power drawn by the load even in steady state is also varying periodically. Due to this, the DC capacitor voltages both at the rectifier and the inverter side are also varying periodically and to control this voltage around 160 kV (the set point), the controller output is also varying periodically. Thus, although the system is operating at the steady state, the steady state values of different quantities are varying periodically around an average value. The plots of load current and load voltage for one cycle are shown in Fig. 4.7. The results of Fourier analysis are also shown in this figure. These two figures (Fig. 4.6 and Fig. 4.7) clearly demonstrate the feasibility of VSC based HVDC scheme for feeding a passive, variable load.

The simulation results for transient faults are shown in Figs. 4.8 and 4.9. These two figures show the results of 3LG fault at the rectifier side and at the inverter side respectively. From these two figures clearly it is obvious that the controller is able to maintain the stability of the system even with heaviest faults. As before in the last section, results of different asymmetrical faults are not shown here as they are quite similar to the results reported in Figs. 4.8 and 4.9.

Thus, with only one simple PI controller at the rectifier side, the multi-PWM VSC based HVDC link is quite able to supply passive loads, both constant and variable.

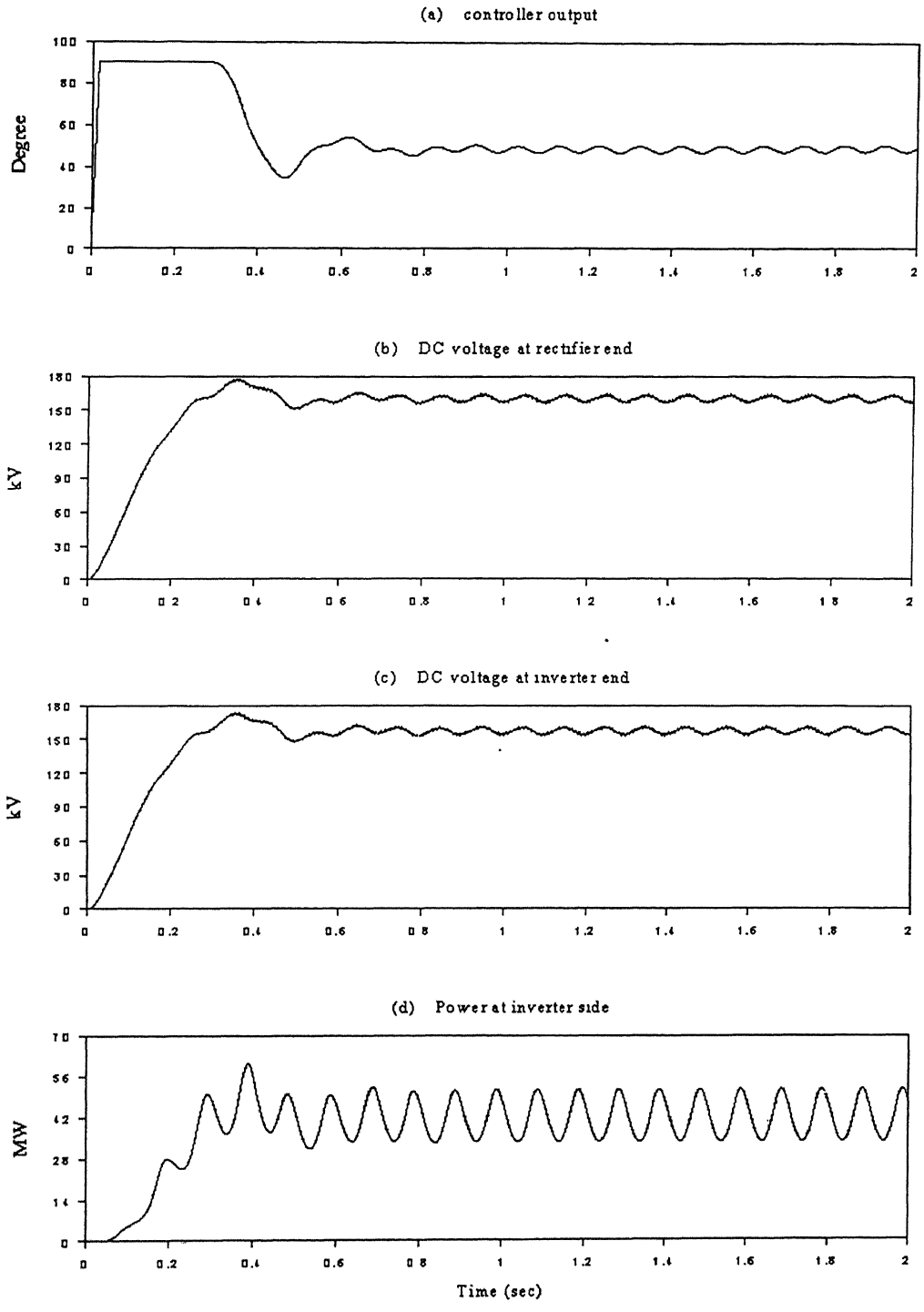

Figure 4.6: Simulation results for variable load at steady state

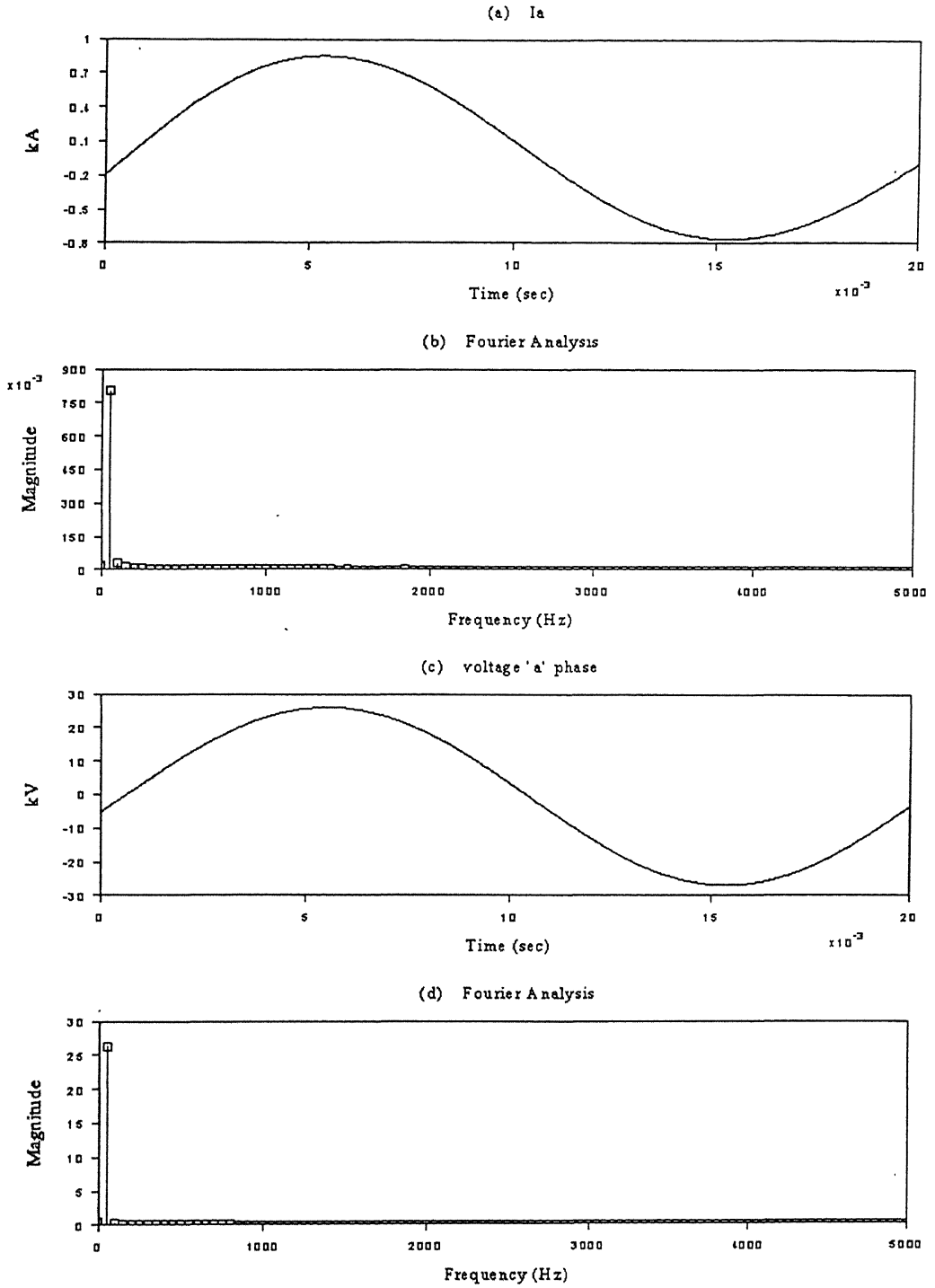

Figure 4.7: Harmonic spectra of the current and voltage at the variable load end

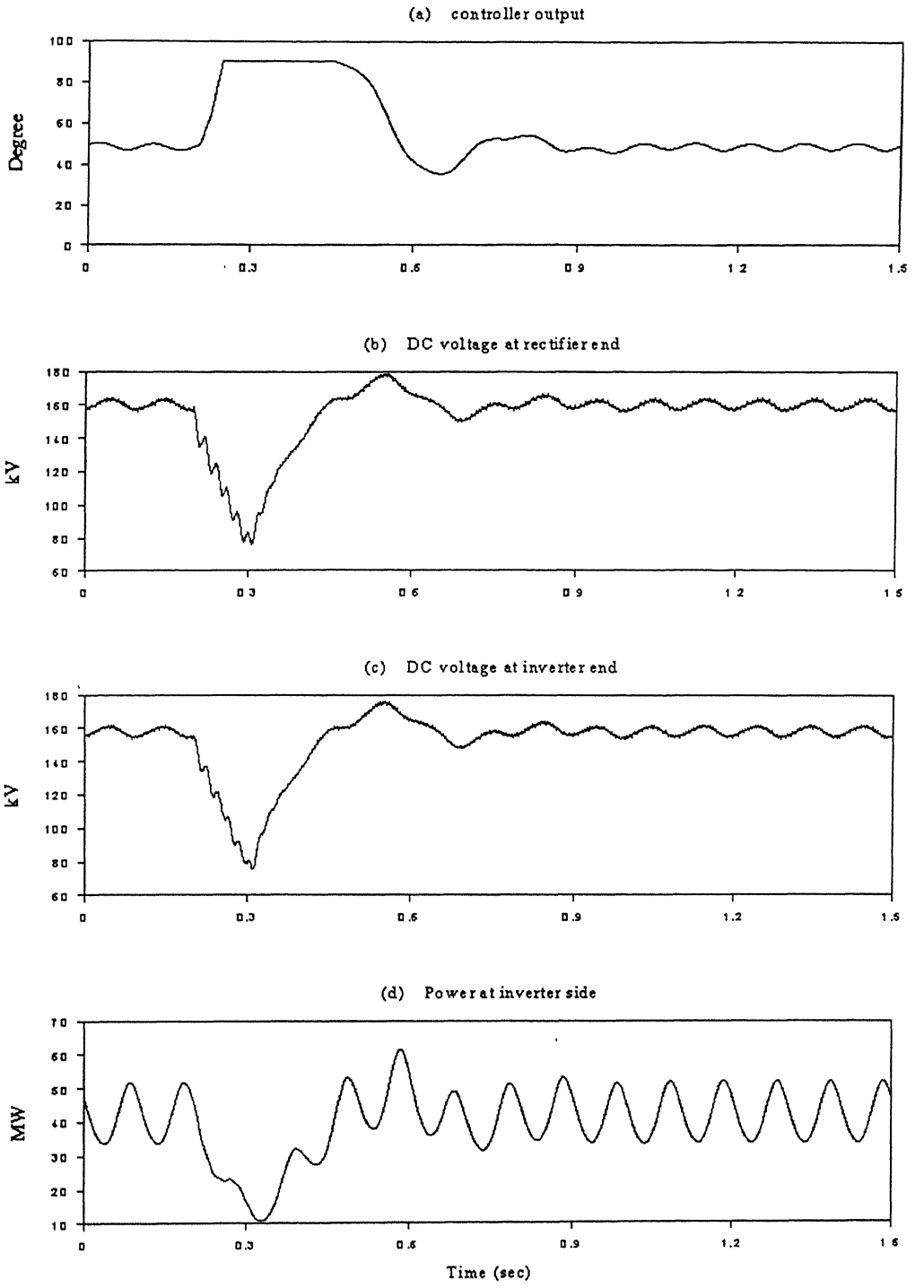

Figure 4.8: Simulation results for the 3LG fault at the AC side of the rectifier station.

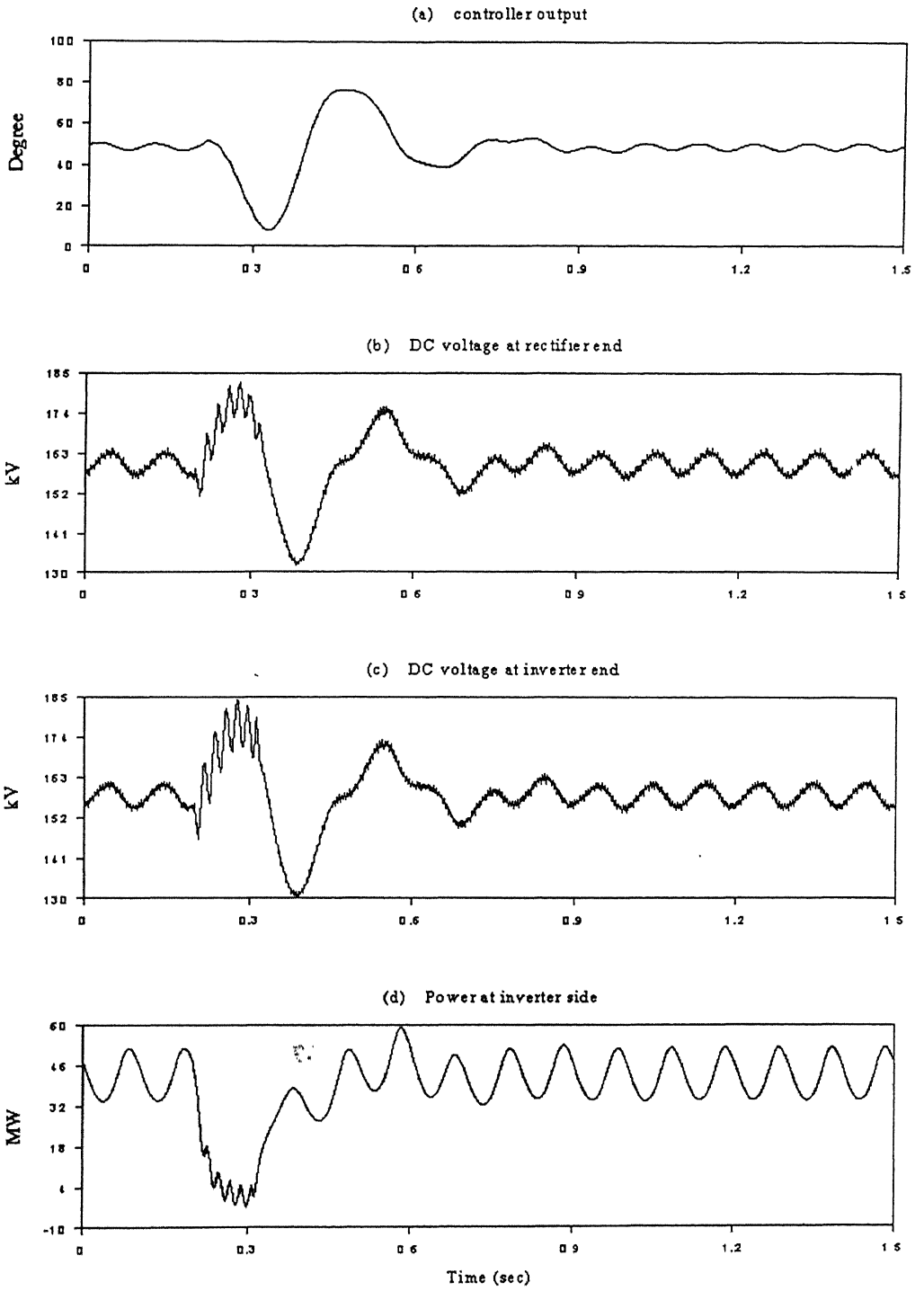

Figure 4.9: Simulation results for 3LG fault at the variable load end.

Chapter 5

CONCLUSION

In this thesis, an investigation has been made regarding the suitable configuration, appropriate control philosophy and applications of force-commutated VSC based HVDC system. The main conclusions of this work are:

(a) For HVDC application, GTO based single-PWM VSC is not suitable from harmonic generation point of view.

(b) GTO based multi-bridge PWM configuration of VSC are quite suitable for HVDC application, as it enables to restrict the switching frequency of individual inverter within allowable limits while achieving very low harmonic content at its output.

(c) For transmission of power between two points in an AC system, one possible control philosophy is to allow the rectifier station to control the DC link voltage while conferring on the inverter station the responsibilities of DC link power.

(d) It is possible to supply passive load by force-commutated VSC based HVDC system.

(e) For supplying passive loads, only voltage control at the rectifier station is sufficient.

Scope of future work

(a) In this work, the parameters of various controllers have been decided by trial and error method. However, there is a need to evolve a systematic mathematical design technique.

(b) Applications of different other VSC configuration, such as multi-level converters can be explored for HVDC application.

(c) An interesting extension of this work would be to investigate the technical feasibility of supplying an arc-furnace load by VSC based HVDC system.

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Appendix

Transformer Specifications :

Connection :	Star / Star
Voltage ratio :	33kV/80kV
MVA rating :	100MVA
Reactance (p.u) :	0.1

Source Specifications :

Voltage rating :	33kV
MVA rating :	100MVA
Source impedance :	1.0Ω